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Development of High-Efficiency Switch-Mode Concurrent Dual-Band RF Power Amplifiers

Yifei Li

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Development of high-efficiency switch-mode concurrent dual-band RF power amplifiers

by

Yifei Li

A dissertation submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering

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ABSTRACT

For the past ten years, we've seen the rapid development of wireless communication along with the number of frequency bands to be supported in a wireless device. RF power amplifiers (PAs), as the last and most important stage in a transmitter, then have to support the increasing number of frequency bands and operation modes. The solution that has been used in industry is simply to increase the number of PAs with each of them covers several adjacent frequency bands. It might be feasible from 2G to 4G since the frequency range is confined within low GHz (<3 GHz), however, as 5G comes, not only the number of frequency band will keep increasing, but the frequency range will expand to much higher ranges (~6 GHz, 30 GHz, 60 GHz, etc.). Higher frequency range will need much more PAs and thus make the traditional solution impractical due to constrained cost and area. In addition, carrier aggregation technique used in 4G and future 5G requires additional filters (diplexer/triplexer) to combines different single-band PAs which will introduce extra power loss.

Multi-band PAs that are able to operate at several frequency bands (not adjacent to each other) simultaneous could potentially reduce the number of PAs and filters thus making the increasingly complicate RF front end feasible in terms of area and cost with reduced power loss. Such PAs are defined as concurrent multi-band PAs. Unfortunately, traditional multi-band PAs were designed for operate one band at a time and thus experienced significant efficiency and output power drop when operate concurrently. A few concurrent dual-band PAs were designed in recent years targeting concurrent operation. However, the drop in both efficiency and output power were still too much to make those PAs useful in actual applications.

The performance of existing concurrent dual-band PAs are mainly limited by their linear-type topology. In this thesis, a switch-mode concurrent dual-band PAs was developed for the first time which, as expected, could achieve higher efficiency with minimum drop in both efficiency and output power.

A concurrent dual-band current-switching class-D PA was proposed in this thesis, and developed from fundamental theories, design methodology, to actual implementation and finally measurement results. The theoretical analysis showed that, the proposed PA could provide a concurrent-mode (two carriers simultaneously) drain efficiency of 87% at 6 dB over drive which was only 5% lower than single-mode operation (one carrier at a time). A concurrent dual-band class-B PA (one of linear-type PAs) on the other hand only have a maximum concurrent-mode drain efficiency 62.5%, 16% lower than single-mode case. The output power drop was also reduced from 3 dB in linear-type PAs to 1.2 dB in the proposed PA. The design of the proposed PA however was complicated due to a large number of harmonics and intermodulation components (IMs) to be properly terminated at the output. To reduce the design complexity, the tradeoff between number of harmonics/IMs to be properly terminated and efficiency was discussed based on ADS simulation. It was found out that, the 2nd harmonics and IM2 were critical to maintain high efficiency, 3rd harmonics and IM3 however had smaller effect on efficiency thus can be neglected (partially) to greatly reduce design complexity with tolerable efficiency degradation. The bias effect was also explored and was suggested that the PA should be bias into triode (defined in Chapter 4) or in other words, bias above class A, in order to achieve high efficiency.

The proposed PA was implemented in a push-pull structure which need a balun at both output and input. The design equations of balun were derived in this thesis together with some

parameter optimization for minimum imbalance and largest bandwidth. The output balun provides not only differential to single-ended conversion but also a 1:4 impedance transformation. The final PA was fabricated and measured in lab. A drain efficiency of 60% was achieved when operating concurrently at 880 MHz and 1.49 GHz with less than 0.5 dB output power drop compared single-mode operation. The performance was among the best concurrent dual-band PAs. Measurement results together with simulation results show that the proposed PA has the ability to achieve much higher efficiency than linear-type concurrent dual-band PAs with minimum efficiency and output power drop, and thus is capable to make increasingly complicated RF FEM feasible.

CHAPTER 1. INTRODUCTION

1.1. Background

A radio-frequency power amplifier (RFPA or simply PA) is the last stage in a transmitter and is used to drive the antennas. It is the most power- and area-consuming block in the whole wireless connectivity part of a wireless device (for example, a cellular phone) [1-4]. Fig. 1-1 shows a typical wireless connectivity part of a cellular phone where necessary filters (duplexer/diplexer) are included between PAs and antennas for band selection and interference suppression. The functionality of RFPA is to amplify low-power signals from the baseband processor/RFIC (Fig. 1-1) to a power level that is large enough to travel the required distance in the air. The typical output

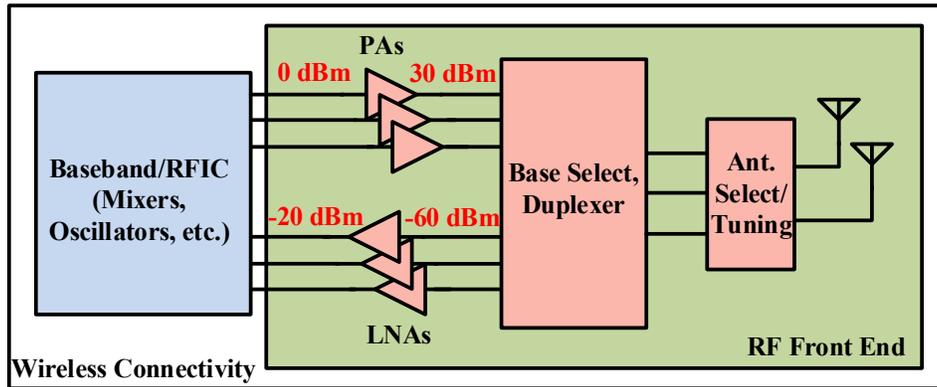


Fig. 1-1 Schematic of the wireless connectivity part of a Cellular phone

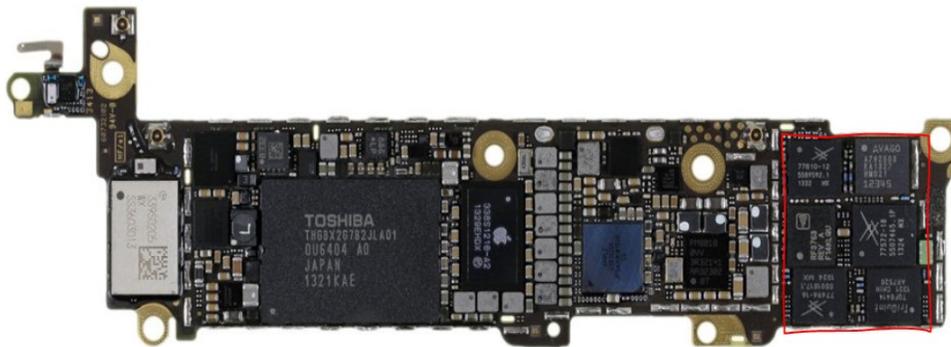


Fig. 1-2 PCB of an iPhone5 [5]

power in a cellular phone is above 1W (30dBm) in order to communicate with the base stations. RFPA are thus one of the most power-consuming blocks in the transceiver and the efficiency of the RFPA largely determines the battery life of a cellular phone. Fig. 1-2 shows the PCB of an iPhone 5 [5], where RFPA are marked using a red rectangle. It can be seen that the total area of RFPA takes up a large portion of the PCB.

The large power consumption and area of RFPA make them the most challenging design block in a wireless device since available battery capacity and area are limited. As wireless standards keep evolving, an increasing number of frequency bands and complexity of modulation schemes make RFPA design more challenging. For example, the number of bands has increased from 13 in 2G GSM to 54 in 4G LTE, and may have another big increase in the coming 5G [6, 7]. The current solution in industry to support this large number of bands is to use multiple wideband PAs (about 10% of fractional bandwidth), each covering several contiguous bands [8]. Fig. 1-3 shows a conceptual RF front end with single-band RFPA in a smartphone, where each RFPA

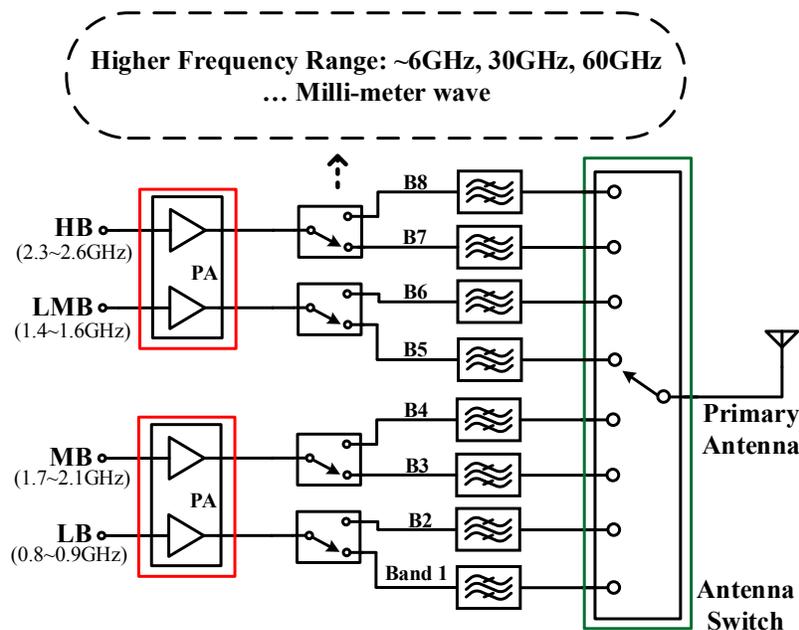


Fig. 1-3 Conceptual RF front end in a smartphone with single-band PAs

covers two adjacent bands within each band group. Band groups are those frequency ranges where frequency bands are clustered. In LTE, there are four band groups called low band (LB), low-mid band (LMB), middle band (MB), and high band (HB), as shown in Fig. 1-3(a). Such a solution will soon become impractical because the number of single-band RFPAs will increase rapidly as frequency ranges expand from lower GHz (~2.6 GHz) in LTE to higher GHz (~6GHz) and eventually to the millimeter range in 5G.

Moreover, carrier aggregation has been introduced as part of the LTE-A standard as a means to provide the increased data rates required by new, intelligent applications [9-11]. So, in addition to supporting different communication bands individually, transmitters supporting carrier aggregation must additionally be able to simultaneously transmit on multiple, possibly disjointed, carrier frequencies. Fig. 1-4 shows a concept of carrier aggregation where five frequency bands each with 20 MHz bandwidth are used to form an effective 100 MHz total bandwidth for the same data transmission. While the data rate could increase tremendously with carrier aggregation, it brings new design challenge to RF front end modules and RFPAs. Such a challenge comes from inter-band carrier aggregations [12] where extra filters/diplexers are needed to provide isolation

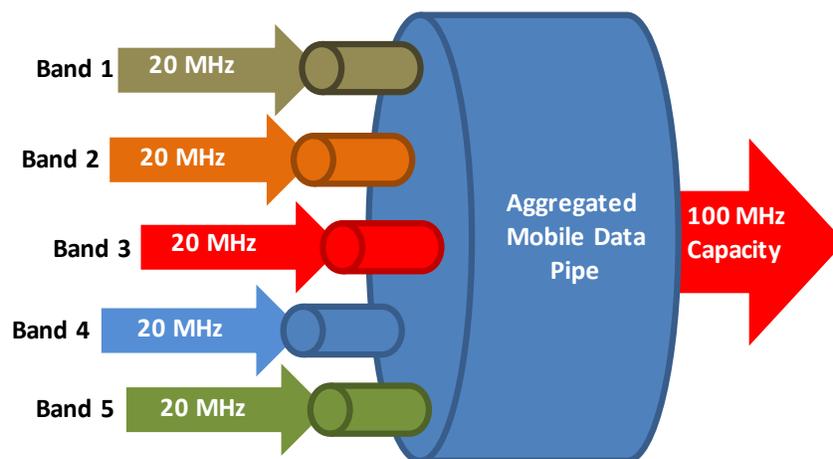


Fig. 1-4 Concept of carrier aggregation

between different bands, as shown in Fig. 1-5 [13, 14], which not only increase the number of filters in the front end module but also introduces extra power loss [15, 16]. With frequency ranges expanding to higher frequencies in the next-generation wireless communication, not only will the number of PAs increase rapidly, as discussed before, but the filters will increase even more than PAs because of carrier aggregation.

Multi-band RFPA that are able to support different band groups can be good candidates to solve the above problem, as shown in Fig. 1-6. With the use of multi-band RFPAs, single-band RFPAs that are working at different band groups can be combined into one power amplifier, thus

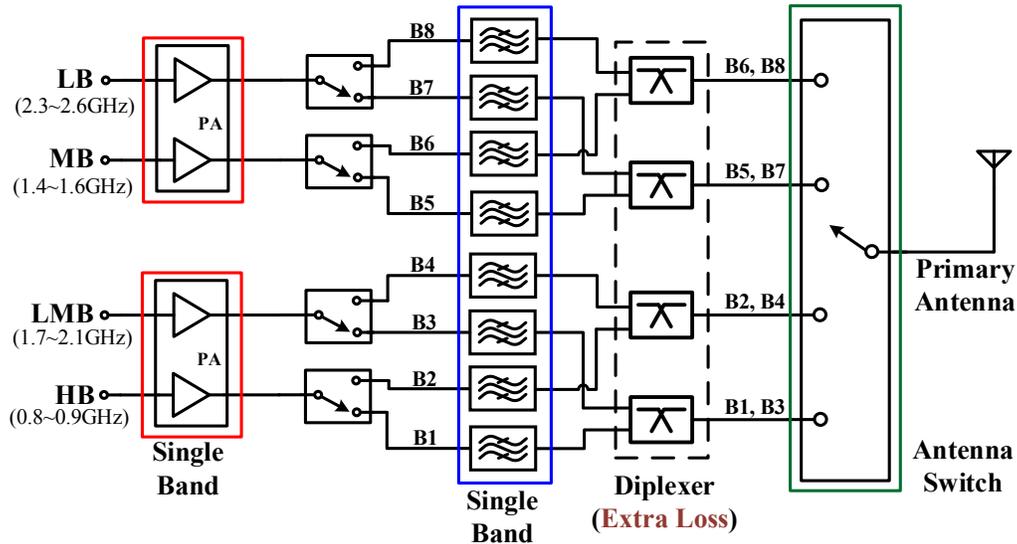


Fig. 1-5 Inter-band carrier aggregation

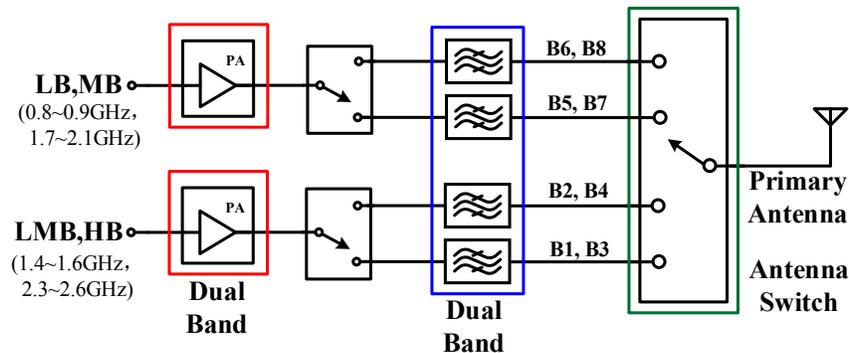


Fig. 1-6 Conceptual RF front end in a smartphone with dual-band PAs

not only reducing the number of PAs, but also eliminating the use of diplexers, since carrier aggregation happens in one power amplifier. Significant space can be saved with the use of multi-band FRPAs. Extra power loss introduced by a diplexer can also be avoided, which will potentially improve the overall efficiency of the whole RF front end.

Those multi-band RFPAs in Fig. 1-6 should be able to operate simultaneously at different frequency bands. Such an operation is defined as a concurrent operation or concurrent mode and such RFPAs are defined as concurrent multi-band power amplifiers. Conventional multi-band PAs were the most straightforward candidates for concurrent multi-band PAs and were first tried out for concurrent operation [17-23]. However, they experienced significant efficiency and output power drop when operated in concurrent mode since they were designed for non-concurrent operation and were not truly concurrent multi-band PAs. The mechanism behind this degradation was largely unexplained until recently, when researchers presented a detailed efficiency analysis of concurrent dual-band linear PAs. It was demonstrated that concurrent dual-band linear PAs, though were designed for concurrent operation, still suffered from large efficiency and output power drops. A detailed literature survey and derivation for concurrent dual-band linear PAs will be presented in Chapter 3.

1.2. Contribution of This Thesis

Traditionally, the relatively low efficiency of linear PAs was overcome through the use of switch-mode PAs. The theoretical understanding and modeling of switch-mode PAs is well understood for single-band operations, but the application of this understanding does not directly lead to optimal designs for concurrent dual-band PAs. This is primarily due to the fundamental difference between how the transistor responds to the input signal. In order to begin to address the

lack of a fundamental understanding of the operation of concurrent multiband switch-mode PAs, this thesis presents the first detailed analysis of a concurrent dual-band class-D PA. In particular, an accurate, idealized model of a switch-mode concurrent dual-band PA is presented and then used to derive general expressions for the maximum theoretical drain efficiency and output power. It is proved that much higher drain efficiency than concurrent dual-band linear PAs, with smaller efficiency and output power drop compared to single-band case, can be achieved. In addition, this thesis presents a detailed discussion of the termination requirements for such a PA and the effects of improper terminations on efficiency. Gate bias effect is also discussed to show the importance of DC operating point. Finally, a concurrent dual-band class-D PA operating at 880 MHz and 1.49 GHz was implemented to validate the theoretical derivation and analysis.

1.3. Organization of This Thesis

This thesis is organized as the follows, Chapter 2 provides the fundamental knowledge of power amplifiers needed in this thesis. In Chapter 3, a thorough literature survey about concurrent dual-band power amplifiers is presented. It will be shown mathematically that significant efficiency and output power degradation exist in concurrent dual-band linear PAs. Chapter 4 then develops a concurrent dual-band switch-mode (class-D) PA that has the ability to achieve much higher efficiency and output power than linear concurrent dual-band PAs and has comparable efficiency to its single-band counterpart. Chapter 5 presents the implementation and measurement results of proposed PA to verify the theoretical analysis. In Chapter 6, potential future work about linearity issues and linearity enhancement is presented. Finally, this thesis is concluded in Chapter 7.

CHAPTER 2. REVIEW OF BASIC POWER AMPLIFIER THEORY

2.1. Introduction

In this chapter, necessary basic knowledge about RF power amplifiers will be provided to help understand the analysis that will be presented in Chapters 3 and 4. In particular, a detailed description and derivation of an idealized, single-band, current-switching class-D power amplifier will be presented to support the analysis of concurrent dual-band class-D PA in Chapter 4. The class-F PA was categorized into a different type of switch-mode PA in many books, journal publication, and other places, however it is the practical version of a class-D PA as will be discussed in this chapter. Based on the theoretical analysis of the class-D PA, important specifications of power amplifiers, such as efficiency (drain efficiency and PAE), output power, linearity, power gain, and bandwidth will be introduced. An important aspect of RFPA design is to make good tradeoffs between those specifications according to different applications. The last part of this chapter will introduce GaN technology, which is used in the proposed RFPA design. GaN power amplifiers have attracted a lot of attention recently, especially for high-power application because of its high breakdown voltage. However, its reliability and cost need to be solved before GaN technology can be widely used.

2.2. Review of Basic Class-D Power Amplifier Theory

Power amplifiers can be divided into two big categories, linear power amplifiers and switch-mode power amplifiers. Linear PAs includes class-A, class-B, class AB, class-C, and class-J PAs [24]. This type of PA operates right below compression in order to avoid nonlinear effects caused by PA compression. Linear PAs are used when linearity is a critical requirement. Switch-

Table 2-1 Comparison of Different PA Topologies

	Type	$P_{out}(W)$	Drain Efficiency	Gain (dB)
Class A	Linear	1	50%	0
Class B		1	78.5%	-3
Class C		0~1	78.5%~100%	$-\infty \sim -3$
Class-D	Switch	$4/\pi$	100%	Compressed
Class E		0.4214	100%	
Class F		$4/\pi$	100%	

mode PAs, on the other hand, work in the overdrive region where PAs are compressed into hard saturation [25], and contains class-D [24-29] , class-F [24, 25, 30-44] and class-E [25, 45-49]. Switch-mode PAs are able to provide higher efficiency and output power compared to linear power amplifiers, except for class-E PAs, but they are naturally nonlinear and need extra treatment to restore linear performance. Table 2-1 shows a comparison of linear PAs and switch-mode PAs in terms of drain efficiency, output power, and power gain, compared to a class-A PA. It can be seen from Table 2-1 that class-D and class-F PAs have the ability to improve both efficiency and output power, and are thus chosen in this thesis for concurrent dual-band switch-mode PA development. Theoretical analysis and derivation will be carried out based on class-D topology as a class-F PA is the practical version of a class-D PA.

2.2.1. Idealized Analysis and Derivation of Single-Band Class-D PA

A class D power amplifier is further divided into two topologies, a voltage-switching class D (VSCD) PA and a current-switching class-D (CSCD) PA. Only the CSCD will be derived in this chapter since the concurrent dual-band class-D PA in Chapter 4 uses current-switching

structure. The VSCD, on the other hand, will be discussed qualitatively. Fig. 2-1 shows the schematic of a typical CSCD PA where both transistors are treated as ideal switches with instantaneous turning on and off. The transformer is also assumed to be ideal in that it has a coupling factor of 1 ($n=2m$) with perfect magnitude/phase balance and infinite bandwidth. The output shunt resonator (L_o , C_o) resonates at a fundamental frequency with a high Q and provides a near short circuit to all harmonic frequencies so that only the fundamental component in the transformer output current (I_T) can flow to the load resistance R_L . During the first half cycle ($0\sim\pi$) when the top transistor (M1) is on and the bottom transistor (M2) is off, the constant DC current (I_{DC}), supplied from the power supply through a choke inductor, is switched to M1. During the next half cycle ($\pi\sim2\pi$), M2 is turned on and M1 is off, the DC current then gets switched to M2. The resultant drain currents, I_{DSP} and I_{DSM} are shown in Fig. 2-2 and are expressed as follow:

$$I_{DSM} = \begin{cases} 0, & 0\sim\pi \\ I_{DC}, & \pi\sim2\pi \end{cases} \quad (2-1)$$

$$I_{DSP} = \begin{cases} 0, & 0\sim\pi \\ I_{DC}, & \pi\sim2\pi \end{cases} \quad (2-2)$$

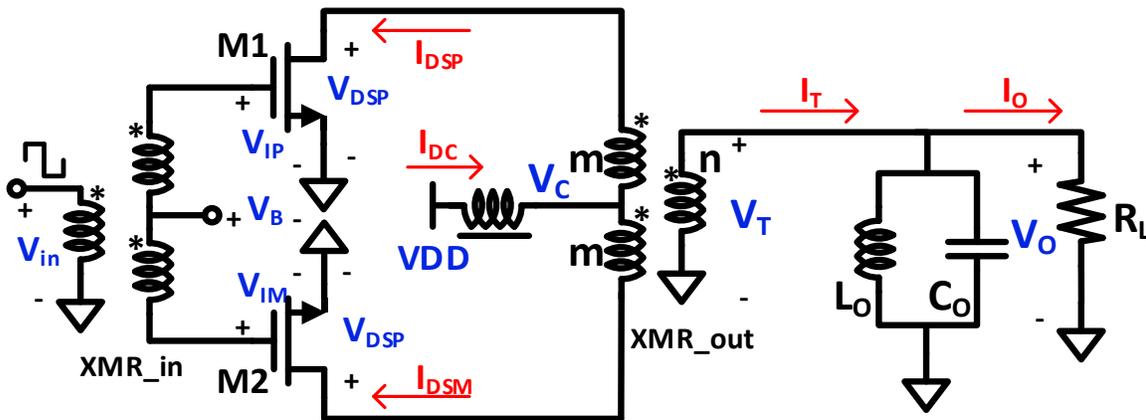


Fig. 2-1 Schematic of current-switching class-D PA

The square waveform is combined through the transformer differentially and forms the transformer output current:

$$I_T = -(I_{DSP} - I_{DSM})/2$$

$$= I_1 \cos(\omega_0 t + \theta_1) + \sum_{n=2}^N I_{2n-1} \cos((2n-1) \cdot \omega_0 t + \theta_{2n-1}), \quad (2-3)$$

where I_1 and I_n denotes the magnitude of fundamental and harmonic currents respectively, while θ_1 and θ_n are corresponding initial phases, and ω_0 is the fundamental frequency. The fundamental components then flow to the load (I_o) and the harmonics are shorted to ground through the shunt resonator (L_o, C_o). The magnitude of fundamental components in the square wave current, (I_T), is $4/\pi$ times larger than the magnitude of the square wave (I_{DC}):

$$I_1 = 4/\pi \cdot I_{DC}/2, \quad (2-4)$$

The output voltage now can be calculated by multiplying I_o and load resistance:

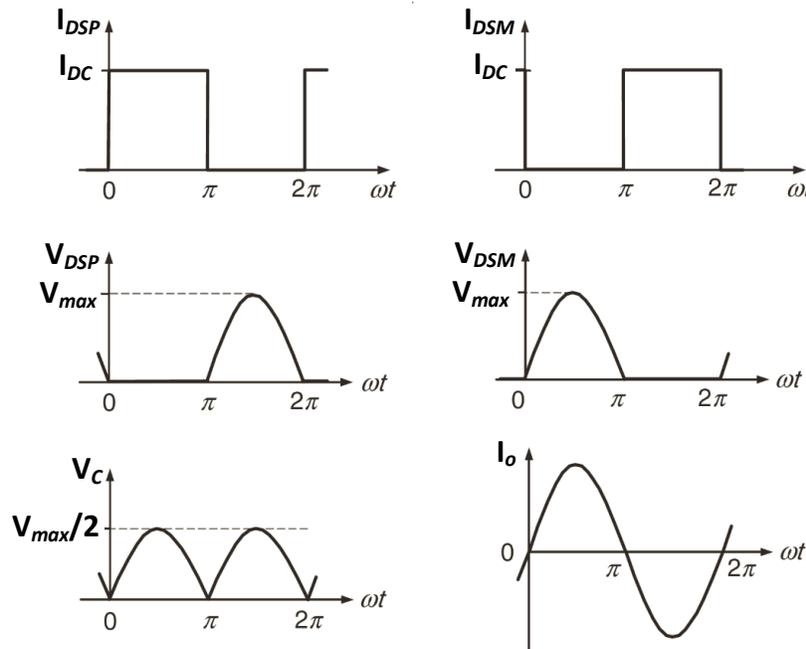


Fig. 2-2 Waveforms in the of current-switching class-D PA [25]

$$\begin{aligned}
V_o &= I_o \cdot R_L \\
&= I_1 \cos(\omega_0 t + \theta_1) \cdot R_L \\
&= V_{max} \cdot \cos(\omega_0 t + \theta_1), \tag{2-5}
\end{aligned}$$

which is a pure sinusoidal waveform and is in phase with I_T while out of phase with I_{DSP} . The output voltage is then coupled back to the drain node of the transistors through the transformer and forms drain voltages as shown in Fig. 2-2. The drain voltages (V_{DSP} and V_{DSM}) are half-wave rectified versions of the output voltage with zero knee voltage (V_{sat}). During the first half cycle ($0 \sim \pi$) when the top transistor (M1) is on and the bottom transistor (M2) is off, the drain voltage of the top transistor, V_{DSP} , stays at zero if the on resistance of the transistors is assumed to be zero. The drain voltage of the bottom transistor, V_{DSM} , on the other hand, has a half-sinusoidal waveform. During another half cycle ($\pi \sim 2\pi$) where M2 is turned on and M1 is off, the shape of V_{DSP} and V_{DSM} interchanges. The complete cycle forms a pure sinusoidal waveform on the balanced nodes of the transformer which is reflected back from the output voltage. The drain voltages also contains harmonics and can be expressed as:

$$V_{DSP} = V_1 \cos(\omega_0 t + \theta_1) + \sum_{n=1}^N V_{2n} \cos(2n \cdot \omega_0 t + \theta_{2n}), \tag{2-6}$$

$$V_{DSM} = V_1 \cos(\omega_0 t + \theta_1 + \pi) + \sum_{n=1}^N V_{2n} \cos(2n \cdot \omega_0 t + \theta_{2n} + 2n \cdot \pi). \tag{2-7}$$

where the magnitude of fundamental components, V_1 , is half of the magnitude of V_{DSP} or V_{DSM} since they are half-wave rectified sinewaves:

$$V_1 = \frac{V_{max}}{2}, \tag{2-8}$$

The drain efficiency of the above CSCD PA is now ready to be calculated. The definition of drain efficiency is the ratio of total output power to total RF DC power:

$$\eta = \frac{P_{out}}{P_{DC}}. \quad (2-9)$$

where output power (P_{out}) is the power delivered to R_L , and DC power (P_{DC}) is the power provided by power supply. Output power is calculated as:

$$P_{out} = \frac{V_{max} \cdot I_1}{2}. \quad (2-10)$$

While total DC power can be calculated as:

$$P_{DC} = V_{DD} \cdot I_{DC}, \quad (2-11)$$

where I_{DC} is pre-defined and V_{DD} is equal to the average value of the transformer center-tap voltage (V_C):

$$\begin{aligned} V_{DD} &= \frac{1}{T} \int_0^T V_C(t) dt \\ &= \frac{1}{2T} \int_0^T (V_{DSP} + V_{DSM}) dt \\ &= \frac{1}{\pi} \cdot V_{max}, \end{aligned} \quad (2-12)$$

where T is the period of the fundamental frequency. In (2-12), it is shown that the average value of a half-wave rectified sine wave is $1/\pi$ of its peak value (V_{max}). Finally, the drain efficiency can be obtained:

$$\begin{aligned}
\eta &= \frac{P_{out}}{P_{DC}} \\
&= \frac{\frac{V_{max} \cdot I_1}{2}}{V_{DD} \cdot I_{DC}} \\
&= \frac{\frac{1}{2} \cdot V_{max} \cdot \frac{4}{\pi} \cdot \frac{I_{DC}}{2}}{\frac{1}{\pi} \cdot V_{max} \cdot I_{DC}} \\
&= 100\%. \tag{2-13}
\end{aligned}$$

The theoretical maximum drain efficiency that can be achieved with a current-switching class-D PA is 100%, as indicated by (2-13). It however requires some idealized assumptions, including instantaneous switching of the transistors, zero knee voltage ($V_{ds,sat}$), and ideal shunt resonator (L_o, C_o) with infinite Q and zero loss.

A voltage-switching class D (VSCD) PA is the counterpart of a current-switching class D PA in that their harmonic termination schemes, collector currents, and voltage waveforms are interchanged. Fig. 2-3 shows a typical VSCD PA schematic where a series resonator (L_o, C_o) is connected to R_L in a series, forcing a sinusoidal output current (I_o) instead of sinusoidal output voltage in a CSCD PA. Another difference from a CSCD PA is the center tap of the transformer. In a CSCD PA, the center tap current is fixed at I_{DC} by a choke inductor, while in a VSCD PA, the fixed item become the center-tap voltage and is fixed by V_{DD} . The center-tap current in a VSCD is no longer a constant. The constant center-tap voltage is steered between the top and bottom transistors as they are turned on and off, resulting in a voltage-switching behavior as shown in Fig. 2-4. The drain efficiency is also 100%, following the similar analysis as presented in the CSCD PA [25].

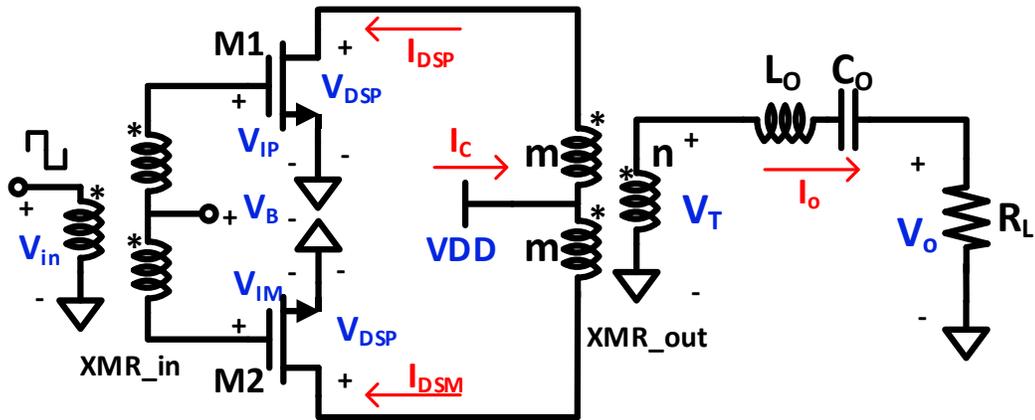


Fig. 2-3 Schematic of voltage-switching class-D PA

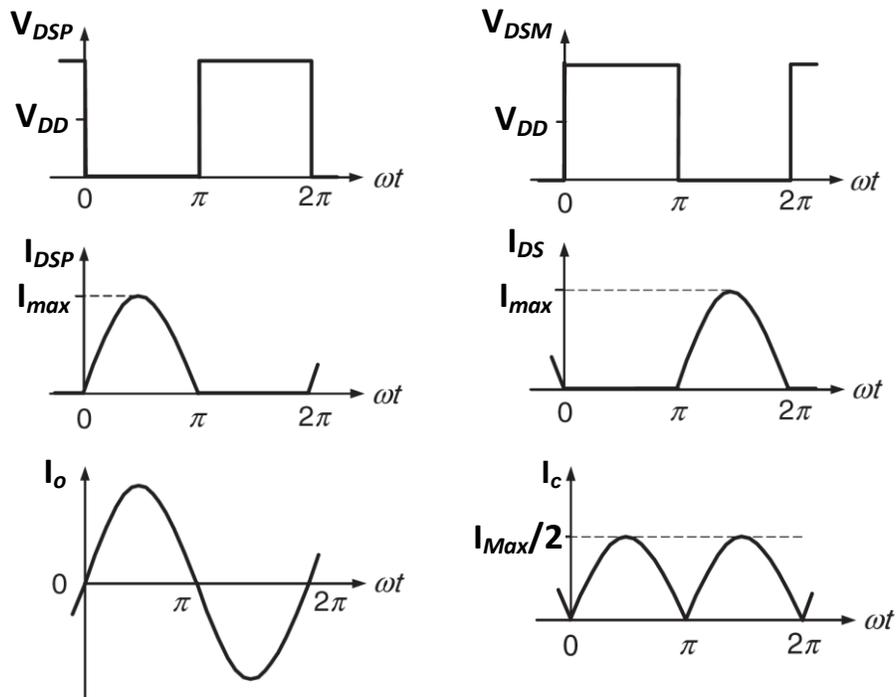


Fig. 2-4 Waveforms in the of voltage-switching class-D PA [25]

2.2.2. Practical Considerations

The derivation of the CSCD PA presented in the above section assumes a zero knee voltage ($V_{ds,sat}$), which however is not realistic. In fact, the finite knee voltage in actual PAs has a big

effect on the drain efficiency and should always be considered. The finite knee voltage in a CSCD PA analysis is usually included as a constant, as shown in Fig. 2-5. The inclusion of knee voltage results in changes in the expression of output power, DC power, and drain efficiency:

$$P_{out} = \frac{(V_{max} - V_{ds,sat}) \cdot I_1}{2}, \quad (2-14)$$

$$V_{DD} = \frac{1}{\pi} \cdot (V_{max} - V_{ds,sat}) + V_{ds,sat}, \quad (2-15)$$

$$\begin{aligned} \eta &= \frac{P_{out}}{P_{DC}} \\ &= \frac{\frac{1}{2} \cdot (V_{max} - V_{ds,sat}) \cdot \frac{4}{\pi} \cdot \frac{I_{DC}}{2}}{\left(\frac{1}{\pi} \cdot (V_{max} - V_{ds,sat}) + V_{ds,sat}\right) \cdot I_{DC}} \\ &= \frac{\frac{1}{\pi} (1 - V_{sat}/V_{ds,sat})}{\frac{1}{\pi} (1 - V_{ds,sat}/V_{max}) + V_{ds,sat}/V_{max}} \cdot 100\%. \end{aligned} \quad (2-16)$$

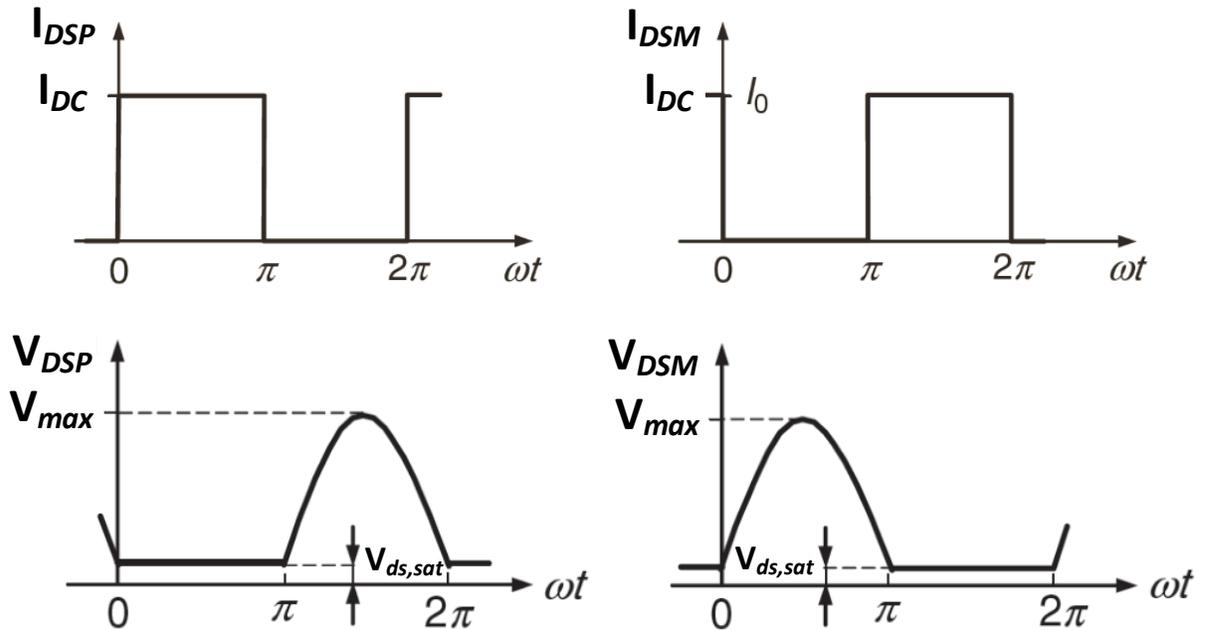


Fig. 2-5 Finite knee voltage in CSCD PAs [25]

It can be seen from (2-16) that drain efficiency decreases as the value of $V_{ds,sat}/V_{max}$ increases. The effects of knee voltage in VSCD PAs are discussed in [25, 26, 41-44]. Due to the effects of knee voltage, CSCD PAs are claimed to have better performance than VSCD PAs [41-44]. The advantages of CSCD mainly come from the fact that transistor output capacitor can be absorbed into the output shunt resonator, resulting a zero-voltage switching (ZVS) feature [26, 27]. However, as the frequency goes higher, this feature becomes more difficult to achieve with the increased inductance introduced by the bond wires.

The second assumption in the idealized CSCD PA derivation is that an infinite number of harmonics are perfectly terminated at the load side. In other words, the output shunt resonator provides an open circuit at the fundamental frequency and a short circuit at all the harmonics. The choke inductor provides an open circuit for all even-order harmonics. Such a load impedance requirement however is not practical. In fact, only up to a 5th-order harmonic can be properly terminated. In most designs, termination up to a 3rd order is enough to provide decent efficiency within a few dB of gain compression [37]. The finite termination of CSCD PA makes it become an inverse class-F PA. The drain efficiency as a function of harmonic termination is thus the same as an inverse class-F PA, as shown in Table 2-2 [30]. The idea of finite termination will also be applied in the design of a concurrent dual-band class-D PA in Chapter 5.

The last assumption in the CSCD PA derivation is the switch model for the transistors. It's assumed that the transistor is turned on instantaneously as provides zero on resistance when input signal or gate-source voltage is above the threshold voltage and turned off immediately when gate-source voltage gets below the threshold voltage. Such an assumption has acceptable accuracy in a single-band class-D PA when the transistor is under enough overdrive (it usually needs to be above

Table 2-2 Drain Efficiency of CSCD PA as a Function of Harmonic Termination

Odd Order	n=1	n=3	n=5	n=∞
m=1	0.5	0.563	0.586	0.637
m=2	0.667	0.75	0.781	0.849
m=4	0.711	0.8	0.833	0.905
m=∞	0.785	0.884	0.92	1.000

Note: n is drain current harmonics, m is drain voltage harmonics

3dB) [25]. In a concurrent operation, however, the assumption becomes inaccurate and needs to be modified. A new model for transistors in concurrent operations will be discussed in Chapter 4.

2.3. Power Amplifier Specifications

2.3.1. Efficiency and Output Power

The main task of a power amplifier is to efficiently generate high levels of output power. The output power level of a power amplifier is determined by the application. For example, output power requirement for cellular phones, WIFI and Bluetooth are 30 dBm, 20 dBm, and 10 dBm, respectively. The output power of a power amplifier is not fixed, but varies as input power changes. Saturated output power however, is limited by supply voltage (V_{DD}) and load impedance (R_L). In the analysis of the CSCD PA in Section 2.2, the saturated output power is determined by:

$$\begin{aligned}
 P_{out} &= \frac{V_{max}^2}{2 \cdot R_L} \\
 &= \frac{(\pi \cdot V_{DD})^2}{2 \cdot R_L}.
 \end{aligned} \tag{2-17}$$

The factor of π is discussed in (2-12). In PA designs, the maximum available power supply is always utilized for better efficiency; R_L is thus easily determined by output power requirement.

In power amplifiers, there are two efficiency definitions, drain efficiency (η) and power added efficiency (PAE). Drain efficiency is defined as the ratio between total output power and total power from DC supply as described in (2-9), which characterizes how much of a portion of the DC power gets delivered to the load. Power added efficiency is defined as:

$$\begin{aligned} PAE &= \frac{P_{out} - P_{in}}{P_{DC}} \\ &= \eta \cdot (1 - 1/G), \end{aligned} \quad (2-18)$$

where G is the power gain. PAE provides a way to characterize how previous stages will affect overall efficiency of the power amplifier. If the last stage of the PA has high enough power gain, then the effect of previous stages is minimum; in another words, PAE is close to drain efficiency. For example, if the power gain is 10dB, which means $P_{in} = 0.1P_{out}$. then $PAE = 0.9\eta$. Under this condition, if we assume the drain efficiency of the previous stage is η_{pre} , then the overall drain efficiency is:

$$\begin{aligned} \eta_{tot} &= \frac{P_{out}}{P_{DC,tot}} \\ &= \frac{P_{out}}{P_{DC} + P_{DC,pre}} \\ &= \frac{P_{out}}{P_{out}/\eta + P_{in}/\eta_{pre}} \\ &= \frac{P_{out}}{P_{out}/\eta + \left(\frac{P_{out}}{G}\right)/\eta_{pre}} \\ &= \eta \cdot \frac{1}{1 + 1/(G \cdot \eta_{pre})}, \end{aligned} \quad (2-19)$$

It can be seen from (2-19) that, as power gain increases, the effect of η_{pre} will have less effect on the overall drain efficiency, η_{tot} . Since PAE and overall drain efficiency both get closer to the drain efficiency of the last stage, PAE can be used to estimate overall drain efficiency. In the rest of this thesis, only the definition of drain efficiency will be used.

The most output power and the best drain efficiency are achieved when a power amplifier is driven into saturation. In the CSCD PA analyzed in section 2.2, the PA is driven to its saturated output power. Only under this condition, 100% drain efficiency can be achieved with proper harmonic termination. When input power is backed off, drain efficiency also decreases. Over drive however, brings nonlinearity issues which is another important specification of power amplifier.

2.3.2. Linearity

Linearity is the one of the most important design specifications in power amplifiers. The pursuit of high efficiency and high output power come after the requirement of linearity. The

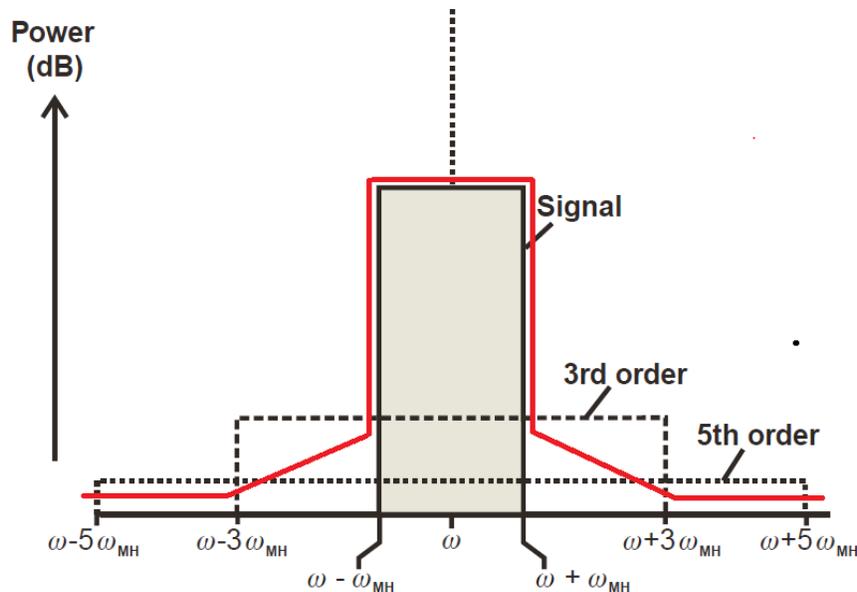


Fig. 2-6 Spectrum regrowth and FCC mask [24]

importance of linearity comes not only from the fact that it will distort baseband signals but also from the emission requirement determined by Federal Communication Commission (FCC), which in most cases is the hardest requirement to meet. In continuous wave (CW) analysis, nonlinearity in PAs causes power suppression on the fundamental tone (characterized with P_{1dB}) and introduces harmonics. Those are not serious problems because harmonics are far away from a fundamental tone and can be easily filtered out either at TX side. Problems come out in the real case when input signals are modulated. The spectrum of such input signals has a certain bandwidth centered around the carrier frequency ω_c . When a modulated signal goes through a nonlinear PA, not only harmonics are generated, but more importantly, extra spectrum will grow around ω_c , with broader bandwidth, as shown in Fig. 2-6. Such a phenomenon is called spectrum regrowth and is caused by odd-order nonlinearities [24]. The widened spectrum can leak into the adjacent channels of the signal and distort the signal in the adjacent channels if they are occupied by other users. In order to avoid such interference, the PA should be linear enough so that the spectrum regrowth is below the FCC mask (the red line in Fig. 2-6).

Nonlinearity in power amplifiers comes from two sources: transistor intrinsic nonlinearity and output clipping (or saturation). Transistor intrinsic nonlinearity includes transconductance, output capacitor, and input capacitor (g_m , C_{out} , and C_{in}). The second nonlinearity, output clipping, only happens when the output signal gets close to a rail-to-rail swing or is driven into saturation, while the former are existing at any signal level. An interesting observation found in [50] showed that the two nonlinear sources above generate 3rd-order nonlinearity in an opposite manner which leads to a null in 3rd-order harmonics or intermodulations (IM3). To explain this, we use simple power series to model PA nonlinearity:

$$V_o = a_0 + a_1V_s + a_2V_s^2 + a_3V_s^3 + a_4V_s^4 + a_5V_s^5 + \dots, \quad (2-20)$$

where V_o and V_s represents output and input voltage respectively. At a low input level, transistor nonlinearity dominates, resulting in a positive 3rd-order coefficient, a_3 , in (2-20). As an input signal increases, nonlinearity caused by output clipping starts to become significant and it assumes a negative a_3 . At a special input level, both nonlinearities have an equal effect and lead to a zero 3rd-order coefficient and thus a null in IM3, as shown in Fig. 2-7. Such an input level is called the “sweet spot” since 3rd-order nonlinearity is the most problematic factor that causes significant spectrum regrowth (Fig. 2-6), as discussed before. The “sweet spot” may be used to achieve very good linearity, however it is limited to very narrow input power range.

The model in (2-20) works well in “weak” nonlinear PAs (usually below P_{1dB}) where phase distortion is not significant. In strong nonlinear PAs, the Volterra series [51-55] should be used to

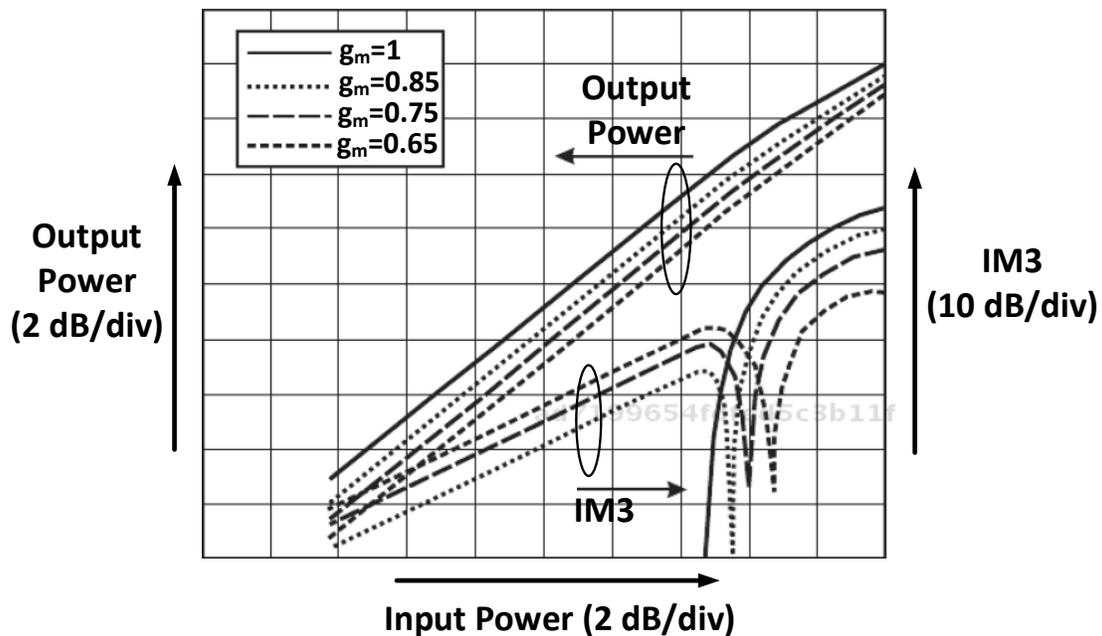


Fig. 2-7 Sweet spot for 3rd-order nonlinearity under different ideal linear transconductance [50]

model the nonlinearity in order to capture phase distortion. However, the Volterra series is not of interest for this thesis and thus is not discussed in detail here.

The non-linear performance of a PA is commonly characterized with AM-AM and AM-PM distortion before testing with modulated data. AM-AM distortion is amplitude-caused amplitude distortion, represented by gain variation as the input power is swept. Gain variation include gain expansion which happens in a lower input power range due to the nonlinearity of g_m , and the gain compression as output starts to approach saturation. Gain expression depends on bias: the more the conduction angle is reduced, the more gain expansion will be observed. Fig. 2-8 shows an example of AM-AM distortion under different gate bias conditions (or conduction angles), which indicates that, as conduction angle reduces, gain expansion becomes more significant and leads to more distortion.

AM-PM distortion is amplitude-caused phase distortion, represented by phase shift variation as input power swept. An example of AM-PM distortion is shown in Fig. 2-9 where the circles indicate 1 dB compression. Though the complete mechanism of AM-PM distortion is not known, some major sources are well recognized. In general, it can be traced to a signal-level dependency of several key transistor model elements, an input voltage dependent input capacitor and resistor, and/or a drain (collector) voltage dependent output capacitor. All of these effects are detailed, interactive, and highly complex in themselves, and pose great challenges for physical modeling. The only way that AM-PM can be treated in a concise manner is to resort to empirical describing functions fitted to physical measurements.

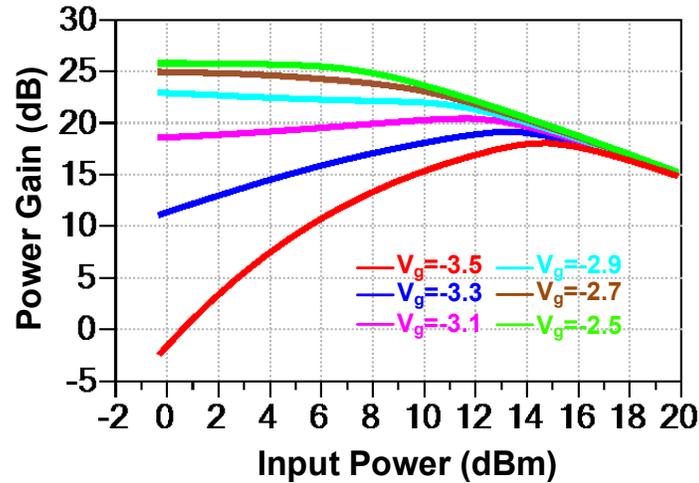


Fig. 2-8 AM-AM distortion under different conduction angles

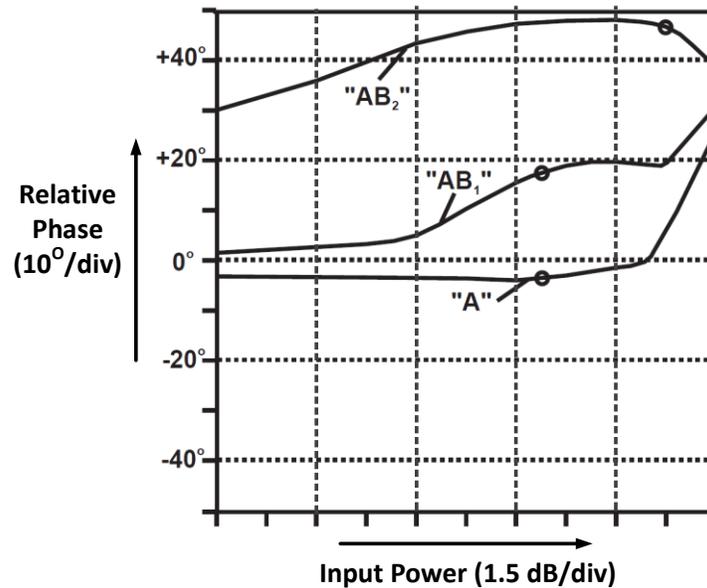


Fig. 2-9 AM-PM distortion under different conduction angles [24]

Power amplifier linearity can be improved simply by backing off output power, but both output power and drain efficiency will decrease. In the class-D power amplifier discussed in this thesis, transistors are overdriven into hard saturation. The nonlinear issue can be solved using LINC techniques which stand for Linear Amplification using Nonlinear Components. LINC technique will be discussed in Chapter 6.

2.3.3. Power Gain and Bandwidth

The requirement of power gain in PA is not as stringent as efficiency, linearity, and output power. However, it is still required to be above 10 dB in order not to hurt power added efficiency (PAE) too much.

The bandwidth in a power amplifier is different from that in an analog circuit. In analog circuits, the bandwidth has a low-pass nature while in PA (or other RF circuits, like LNA), it has a band-pass nature centered around the designed frequency. In general, wide bandwidth is preferred in power amplifiers as they can cover more adjacent bands with one power amplifier. This is especially true as the number of bands keeps increasing, with 5G coming. However, a wide bandwidth usually requires complex matching network design in both output (OMN) and input (IMN), and this would result in a higher insertion loss in the matching networks. On top of this, PA performance (efficiency, gain, etc.) tends to degrade from the optimized center frequency to the edge of the bandwidth. So, if cost is more of a concern than performance, wide-band PAs are preferred; if performance is the priority, then multiple PAs optimized at different center frequencies would be used to cover the same number of bands.

2.4. Review of GaN Technology

Gallium Nitride (GaN) has become a very attractive material for power amplifier design due to its high break down voltage and high power density. Traditional technologies such as CMOS and GaAs suffer from their low break down voltage when used in power amplifiers. CMOS, in particular, failed to be an option to PA designers despite its low cost. A $0.18\mu\text{m}$ CMOS transistor has a breakdown voltage of less than 5 V and a typical supply voltage of 1.8 V. Such low supply becomes closer to knee voltage and thus leads to lower drain efficiency in PAs as shown in (2-16).

Table 2-3 Material property comparison

Material	Band Gap Energy (eV)	Critical Breakdown Field (MV/cm)	Thermal Conductance (W/cm-K)	Mobility (cm ² /V-s)	Saturated Velocity (10 ⁷ cm/s)	Relative Dielectric Constant
Si	1.1	0.3	1.5	1300	1	11.9
GaAs	1.4	0.4	0.5	6000	1.3	12.9
4H SiC	3.2	3.3	3.7	610	2	9.7
6H SiC	3.0	3.0	4.9	310	2	9.7
GaN	3.4	3.0	1.5	1500	2.7	9.0

In addition, low supply voltage requires a small optimal load impedance in order to generate the same output power level. The above 1.8 V V_{DD} will result in an optimal load impedance of only 1.62 Ω in a class-A PA when an output power of 1 W is required. The small optimal load impedance need high-Q matching network which not only increases insertion loss but also reduces the bandwidth.

GaN transistors can provide much higher breakdown voltage due to the wide bandgap of GaN material. Table 2-3 summarize the property of different semiconductor material from which it can be seen that GaN has much higher breakdown electrical field than Si and GaAs which make it a perfect material for power amplifiers. Good thermal conductivity of GaN, and its ability to grow on SiC [56], greatly relieve the thermal issue of power amplifiers. When compared to SiC, which has similar breakdown electrical field and higher thermal conductivity, GaN has much higher mobility. More importance, GaN can be used to fabricate high electron mobility transistors (HEMTs) which can further increase its mobility [56]. High breakdown voltage, high power density, good thermal conductivity and good mobility make GaN HEMTs very good candidate for

microwave power amplifiers, especially concurrent dual-band PAs which have doubled peak drain voltage.

The formation of HEMT using GaN is also easier than using GaAs due to its possibility of inducing a very high concentration of two dimensional electron gas (2DEG) without any layer doping, it only needs the epitaxial growth of an AlGaN layer on top of a GaN buffer, thus removes all the problems related to the intentional doping [57]. Fig. 2-10 shows a cross section of a typical GaN HEMT. The generation of the thin 2DEG comes from the high polarization contribution of each single layer and the heterostructure. Detailed theory is discussed in [56, 57].

GaN HEMT however suffers from a discrepancy between static I-V curve and load-pull measurement, which is also called current collapse [56]. It is believed to be a trap-related phenomenon in both surface and bulk. This problem will limit the microwave output power of GaN HEMT and need to be passivated before it can be used. As a new technology, the reliability of GaN is still not as reliable as GaAs or CMOS. The special treatment and reliability issue of GaN HEMT increases the cost of this technology and make it not widely used yet. However, the trend of GaN HEMT is towards high power, high frequency and improved reliability with lower cost.

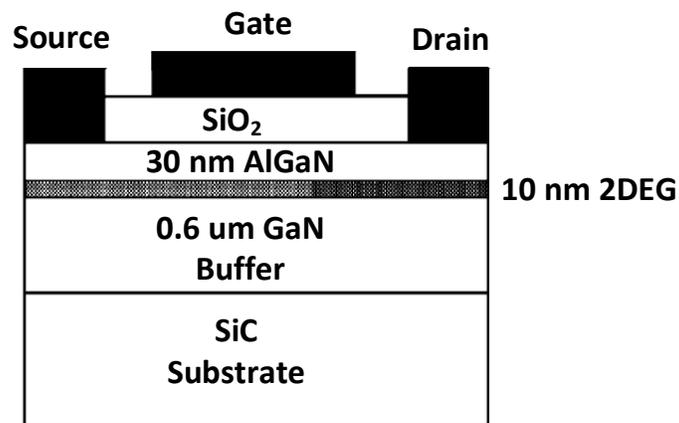


Fig. 2-10 Cross section of a typical GaN HEMT

2.5. Conclusion

A detailed derivation of current-switching class-D PA was presented in this chapter as a perversion for concurrent dual-band class-D PA development. Practical considerations such as knee voltage, finite termination and finite switching time were discussed. Those are important aspects in design of class-D PA and require remodeling in concurrent dual-band class-D PAs. Importance PA design specifications were then presented and their importance and tradeoffs discussed. Finally, a simple review of GaN material and GaN HEMT were provided. GaN HEMT has much higher breakdown voltage than CMOS AND GaAs which make it a good candidate for concurrent dual-band PAs since their peak drain voltage are doubled compared to single-band PAs.

CHAPTER 3. CONCURRENT OPERATION IN LINEAR POWER AMPLIFIERS

3.1. Introduction

It was pointed out previously that carrier aggregation technique, a standard feature in 4G and the next generation standard, brings more challenges for system level design and power amplifier design. As a result, there has been quite a lot of research and discussion at the architecture/system level [58-64]. However, concurrently-operating power amplifiers for carrier aggregation have not attracted a lot of attention until recent years.

The traditional multi-band power amplifier is the first and the most straightforward candidate for concurrent multi-band PAs, but they experience significant drain efficiency and output power drop when working in concurrent mode (operating at multiple frequency bands simultaneously), as discussed in Chapter 1. The reason behind such performance degradation was largely unexplained until recently, when researchers presented a detailed efficiency analysis of concurrent dual-band linear PAs. The major difference or improvement in those concurrent dual-band linear PAs compared to traditional multi-band PAs is that they started to take control of the inter-modulation components (IMs). In traditional multi-band PAs, there are no IM components, since they were designed to operate at one frequency at a time.

Although concurrent dual-band linear PAs are designed for concurrent operation and have good control of IM components, they also suffer from poor drain efficiency and output power drop when compared to their single-band counterparts. It is a serious problem considering the already low drain efficiency of single-band linear PAs. This chapter will first provide a detailed literature

survey of transitional dual-band PAs for concurrent operation and existing concurrent dual-band linear PAs. Then a detailed derivation of concurrent dual-band class-A and class-B PAs will be presented to show the reason for drain efficiency and output power drop.

3.2. Literature Survey on Concurrent Dual-Band Power Amplifiers

Conventional multi-band PAs utilized a tunable load/matching network to realize frequency selection [65, 66]. This type of PA features simple design, potential broad bandwidth, optimized design for each band, and theoretically can support a large number of frequency bands. However, such a load network usually incorporates RF switches and will introduce extra power loss which may easily surpass the benefit brought by optimized design. Thus, the overall efficiency of such PAs is actually lower. In addition, because of the switching nature, they are not able to support concurrent operation (operate more than one frequency simultaneously).

Recognizing the difficulties resulting from the RF switches, [67-71] present load/matching networks that employ high-order resonators that are capable of presenting the necessary impedance to the transistor at multiple bands, simultaneously. The band of operation is selected simply by the frequency of the input signal. When operated one band at a time, these systems have been shown to achieve similar efficiencies when compared to their single-band counterparts. When excited with multiple carrier frequencies simultaneously, however, a significant drop in both efficiency and output power was observed. The mechanism behind this degradation was largely unexplained until recently, when researchers presented a detailed efficiency analysis of concurrent dual-band linear PAs [72-74].

It was realized in [72-74] that inter-modulation components played an important role in concurrent dual-band PAs. The performance degradation of traditional dual-band PAs may be due

to the loss of IM components control. IM components in [72-74] were simply shorted to ground, as required by all linear power amplifiers. Despite the good control of the IMs as well as the harmonics in [72-74], drain efficiency and output drop were still observed in concurrent dual-band linear PAs. The rest of this chapter will present a detailed derivation to show the reason and amount of drain efficiency and output power drop in concurrent dual-band PAs. It was demonstrated that, in concurrent mode operation, the theoretical maximum drain efficiency for dual-band class-A operations is 25% (compared to 50% for single-band PAs) and for class-B the maximum theoretical drain efficiency is only 62% (compared to 78.5% for single-band PAs). Moreover, in concurrent dual-band operations, the output power in each band is reduced by 3 dB, as compared to a single-band PA.

3.3. Analysis of Concurrent Dual-Band Class-A Power Amplifiers

A concurrent dual-band class A-PA has a schematic very similar to a single-band class-A PA, except for the output matching network (OMN) and input matching network (IMN). In a concurrent dual-band class-A PA, the output and input matching networks are able to transform the standard impedance of 50Ω to an optimal load impedance (R_L) at two different operation

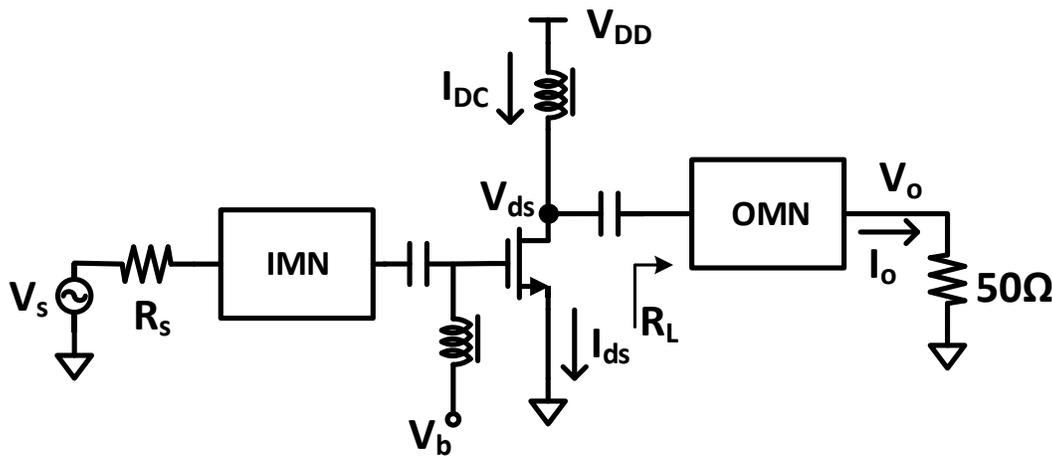


Fig. 3-1 Simple Schematic of a Class A PA

frequency bands without tuning,. while in single-band PAs, the matching networks are only able to transform the impedance at one frequency. Such matching networks are called dual-band matching networks. For simplicity, we do not consider the design of dual-band matching networks in this analysis but assume the optimal load impedance (R_L) is readily available. The schematic of a concurrent dual-band class-A PA is shown in Fig. 3-1, where the optimal load impedance for both frequency bands is the same and denoted as a pure resistance R_L . Parasitic elements of the transistor are not considered here for theoretical analysis purposes. The assumption of equal R_L in both bands is valid when the transistor is assumed to have frequency-independent transconductance.

To start the analysis, we first assume the following input signal:

$$V_{in}(t) = A_L \sin(\omega_L t) + A_H \sin(\omega_H t) + V_b \quad (3-1)$$

where A_L , A_H are the magnitudes of each carrier and are both normalized to 1. V_b is the base bias voltage. The ratio of A_L/A_H can be any value covering a single-mode operation ($A_L/A_H = 0$ or ∞) to a balanced concurrent-mode operation ($A_L/A_H = 1$). Since the worst-case efficiency occurs for a balanced concurrent mode [72, 74], only a balanced concurrent-mode operation is analyzed here. The bias voltage, V_b , guarantees the minimum value of V_{in} to be equal to V_{th} (V_{th} is assumed to be zero in this analysis), as required by class-A PA. In most frequency ratios, ω_H/ω_L , the peak value of two sinusoidal signals added together can be assumed with great accuracy to be 2. However, some special frequency ratios (2, 3, 4, etc.) can result in a peak value that is quite a bit lower than 2 [72, 74]. Generally those frequency ratios should be avoided since there will be quite a number of intermodulation components or harmonics fall onto the two fundamental bands. In

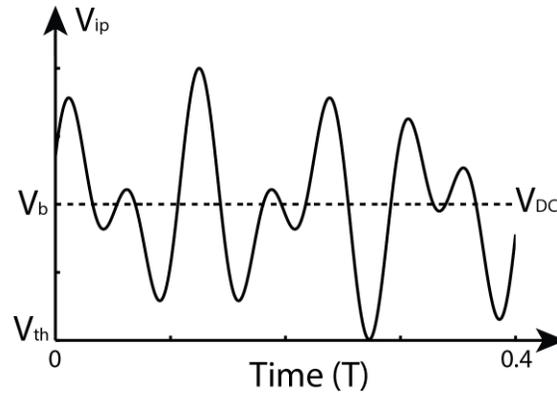


Fig. 3-2 Concurrent dual-band input signal of concurrent dual class-A PA

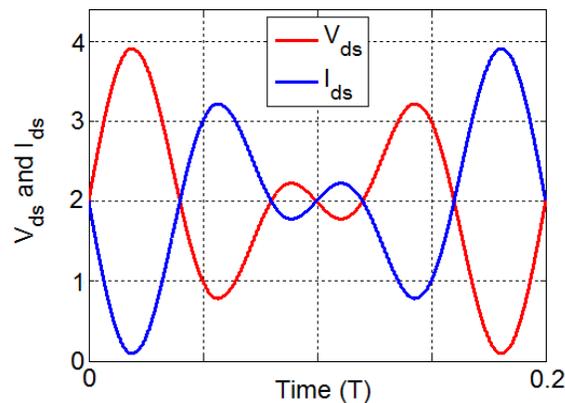


Fig. 3-3 Drain voltage and current waveform of concurrent dual-band class-A PA

this analysis, the peak value and V_b is assumed to be 2. Other than the magnitude of each carrier, the transconductance of the transistor (g_m) and the load impedance (R_L) are also normalized to 1.

Fig. 3-2 plots the waveform of the concurrent dual-band input signal. Unlike a single-band signal, the concurrent dual-band signal, as shown in Fig. 3-2, has a time-varying envelope. For linearity considerations, the peak envelope should be working at the edge of gain compression (no overdrive). The lower envelopes are then working at power back-off regions, which will result in lower efficiency for the concurrent dual-band class-A PAs. One thing worth mentioning is that a concurrent dual-band PA can operate as a single carrier (defined as single mode) as well as operating as a concurrent dual-band carrier (defined as concurrent mode). The single-mode

efficiency and output power would be equal to a single-band PA if losses from matching networks are not considered. It is the concurrent mode that has the significant drop in both efficiency and output power.

As mentioned before, the transistor has a unit transconductance when turned on, which leads to a drain current as expressed below:

$$\begin{aligned} I_{ds}(t) &= g_m \cdot V_{in}(t) \\ &= g_m \cdot (A_L \sin(\omega_L t) + A_H \sin(\omega_H t) + V_b) \\ &= g_m \cdot (A_L \sin(\omega_L t) + A_H \sin(\omega_H t)) + I_{DC}. \end{aligned} \quad (3-2)$$

Where I_{DC} is the DC current from the power supply and is equal to 2. The blue curve in Fig. 3-3 shows the waveform of the current in (3-2), which is the same waveform as the input signal. This is due to the normalized transconductance. The AC component of drain current is delivered to the load and causes a load voltage of:

$$V_o(t) = -R_L \cdot g_m \cdot (\sin(\omega_L t) + \sin(\omega_H t)). \quad (3-3)$$

Where R_L is normalized to 1, as mentioned previously. The drain voltage can then be obtained:

$$V_{ds}(t) = V_{DD} + V_o(t) = V_{DD} - R_L \cdot g_m (\sin(\omega_L t) + \sin(\omega_H t)) \quad (3-4)$$

For maximum output power and efficiency, the drain voltage should swing from 0 to $2V_{DD}$ shown as the red curve in Fig. 3-3. This indicates that:

$$V_{DD} = A_L + A_H = 2. \quad (3-5)$$

Where the knee voltage (V_{sat}) is assumed to be zero. Now the total output power can be calculated:

$$P_{out} = P_{out1} + P_{out2} = \frac{(R_L g_m)^2}{2R_L} + \frac{(R_L g_m)^2}{2R_L} = 1 \quad (3-6)$$

and then the overall drain efficiency:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{R_L * (g_m * A)^2}{V_{DD} * I_{DC}} = \frac{R_L * (g_m * A)^2}{(R_L * g_m * 2A) * (g_m * 2A)} = 25\% \quad (3-7)$$

A 25% drop in drain efficiency is observed, compared to single-band class-A PA (50% drain efficiency). Under the same bias condition (same I_{DC} and V_{DD}), the output power for a single-band class-A PA would be 2, which indicates an output power drop of 3 dB in the concurrent dual-band class-A PA.

It is assumed in above analysis that, the peak value of $\sin(\omega_L t) + \sin(\omega_H t)$ is 2. However, it is not always the case. In fact, the peak value will change as the frequency ratio, ω_H/ω_L changes, and will result in drain efficiency variation. Using above analysis but with V_{DD} equal to half of the actual peak value, the drain efficiency as a function of frequency ratio is plotted in Fig. 3-4. It can

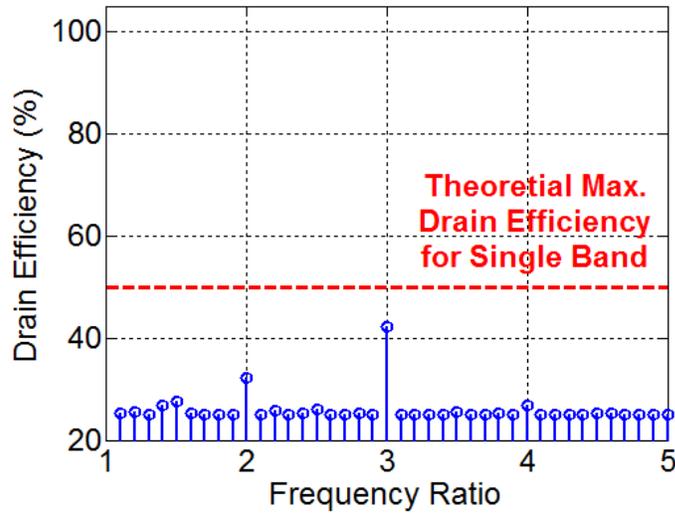


Fig. 3-4 Drain efficiency of the concurrent dual-band class-a PA as a function of frequency ratio

be seen that, except for some harmonic-related frequency ratios, the drain efficiency of a concurrent dual-band class-A PA is 25%, which indicates the correctness of the above derivation.

3.4. Analysis of Concurrent Dual-Band Class-B Power Amplifiers

A concurrent dual-band class-B PA requires a dual-band shunt resonator resonating at the two fundamental frequencies, ω_L , ω_H , to allow only fundamental components to be delivered to the load resistance and short all other harmonics and IM components to ground (Fig. 3-5). As in the analysis of concurrent dual-band class-A PAs, the optimal load impedance (R_L) is assumed to be equal for both bands and is normalized to 1. The transistor does not have any parasitics and has a normalized transconductance when turned on. The knee voltage is again assumed to be zero ($V_{ds,sat}=0$). The input signal is similar to the class-A case however, with zero base bias voltage since the threshold voltage is assumed to be zero in the analysis:

$$V_{in}(t) = A_L \sin(\omega_L t) + A_H \sin(\omega_H t) + V_b \quad (3-8)$$

where $A_L = A_H = 1$ indicating balanced concurrent-mode operation and V_b is equal to zero. Fig. 3-6 plots the input signal where only the part above zero will introduce drain current. Drain current can be expressed as:

$$\begin{aligned} I_{ds}(t) &= \begin{cases} 0, & V_{in}(t) < 0 \\ g_m V_{in}(t), & V_{in}(t) > 0 \end{cases} \\ &= g_m \cdot \frac{|V_{in}(t)| - V_{in}(t)}{2} \end{aligned} \quad (3-9)$$

A portion of the drain current is shown in Fig. 3-7 as a blue curve. Clearly, such a drain current contains only fundamental components and even-order harmonics/IMs due to the absolute value

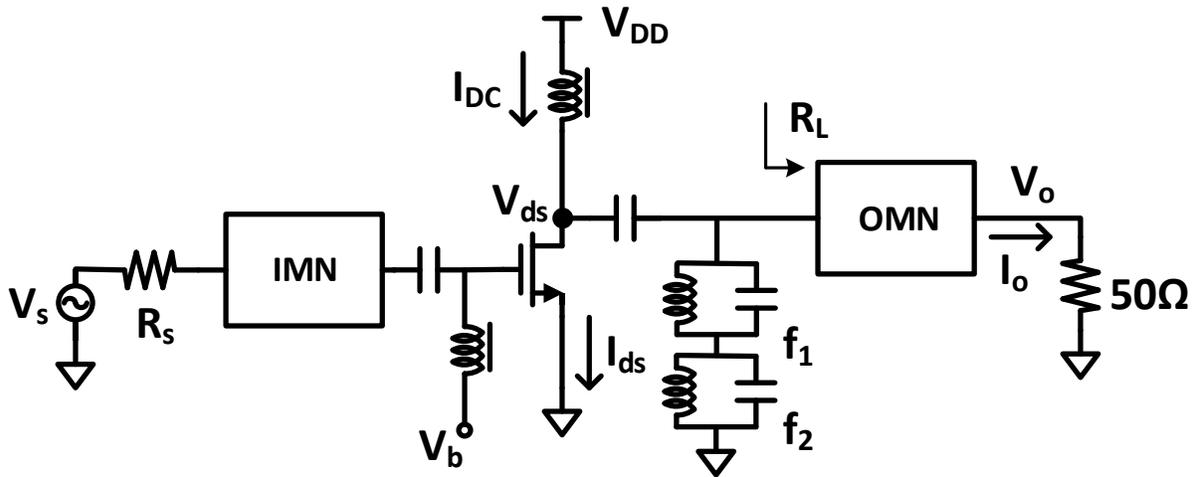


Fig. 3-5 Simple schematic of a concurrent dual-band class-B PA

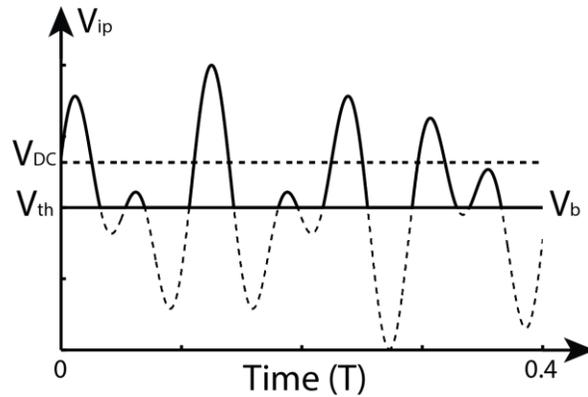


Fig. 3-6 Concurrent dual-band input signal of concurrent dual class-B PA

function in (3-9). The drain current thus can also be expressed using a Fourier series, assuming that ω_L and ω_H have finite beat frequency:

$$I_{ds}(t) \approx \sum_{n=0}^N \sum_{m=0}^M I_{(m,n)} \sin\left((m\omega_L \pm n\omega_H)t + \theta_{(m,n)}\right) \quad (3-10)$$

where m and n are used to index the frequency components (e.g., the fundamentals, IM, harmonics, etc.) of the output current. Other than $I_{(0,0)}$, $I_{(0,1)}$, and $I_{(1,0)}$, which represent the DC and fundamental components respectively, $m + n$ are odd numbers indicating that only even-order harmonics and IM components exist in drain current. Assuming that the dual-band shunt resonator

ideally removes all unwanted frequency components, only the fundamental components of the output current, $I_{(1,0)}$ and $I_{(0,1)}$, flow into the load resistance, R_L . Thus output current can be expressed as:

$$I_o(t) = -(I_{(1,0)} \sin(\omega_L t + \theta_{(1,0)}) + I_{(0,1)} \sin(\omega_L t + \theta_{(0,1)})) \quad (3-11)$$

and the output voltage:

$$V_o(t) = R_L \cdot I_o(t) = -R_L \cdot (I_{(1,0)} \sin(\omega_L t + \theta_{(1,0)}) + I_{(0,1)} \sin(\omega_L t + \theta_{(0,1)})), \quad (3-12)$$

which contains only the two fundamental components because of the output dual-band resonator. To achieve maximum efficiency, drain voltage should swing from 0 to $2V_{DD}$ which results in the following relation:

$$V_{DD} = R_L * (I_{(1,0)} + I_{(0,1)}) = 1 \quad (3-13)$$

Now drain efficiency is ready to be calculated:

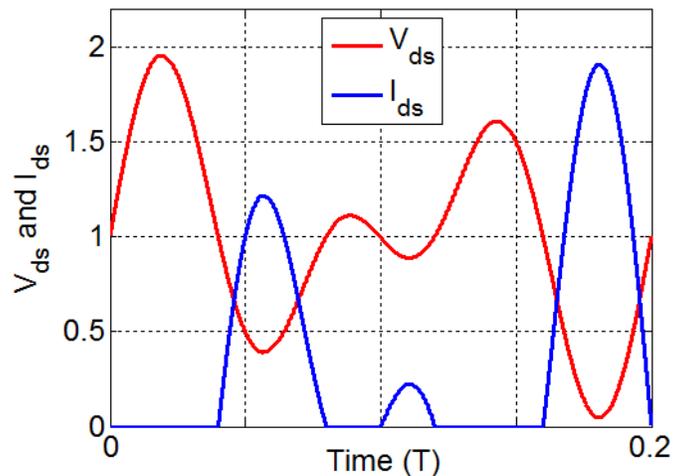


Fig. 3-7 Drain voltage and current waveform of concurrent dual-band class-B PA

$$\begin{aligned}
\eta &= \frac{P_{out}}{P_{DC}} \\
&= \frac{R_L * (I_{(1,0)}^2 + I_{(0,1)}^2) / 2}{V_{DD} * I_{DC}} \\
&= \frac{R_L * (I_{(1,0)}^2 + I_{(0,1)}^2) / 2}{R_L * (I_{(1,0)} + I_{(0,1)}) * I_{DC}} \\
&= \frac{I_{(1,0)}^2 + I_{(0,1)}^2}{2 * (I_{(1,0)} + I_{(0,1)}) * I_{(0,0)}}. \tag{3-14}
\end{aligned}$$

It is very difficult to find the analytical relation between $I_{(1,0)}$, $I_{(0,1)}$, $I_{(0,0)}$, and the peak value of I_{ds} since the peak value and zero-crossing point of I_{ds} change as the frequency ratio varies. Approximation methods exist to find the relation between fundamental components and the DC component [72, 74], but they all end up in great complexity if better accuracy is desired. For the calculation of drain efficiency, a numerical method is good enough. But in order to obtain some insight, such as the magnitudes and positions of different frequency components, approximation methods have to be used.

Here we use numerical methods to calculate drain efficiency. In the calculation, g_m , $A_{L(H)}$, R_L are normalized to 1. V_{DD} is adjusted to be equal to the actual total magnitude of (3-12). The frequency ratio is swept from 1.1 to 5 with 0.1 as steps. The initial phase difference between two carriers is kept at zero. Matlab calculation results are plotted in Fig. 3-8, from which we can see that for most frequency ratios, the drain efficiency is around 62%, 16.5% lower than the single-band case. This efficiency degradation is less significant compared to concurrent dual-band class-A PA. On the other hand, output power has a 3dB drop, compared to the single-band case for most frequency ratios, which is same as concurrent dual-band class-A PA.

Some special frequency ratios exist that yield much higher concurrent-mode efficiency and output power, as shown in Fig. 3.4 and 3-8. However, those frequency ratios are harmonic-related or IM-related and that could cause severe cross interference due to either harmonics or IM components. Those special frequency ratios should generally be avoided in concurrent dual-band PAs. One thing worth noting is that, for other normal frequency ratios, which have a 16% efficiency drop, drain efficiency doesn't have a noticeable change over a sweep of phase, while for those special frequency ratios, drain efficiency is a function of the initial phase, different from the two carriers. We guess this is due to less interference cause by harmonics and IM components; however no analysis has been provided so far to explain this phenomenon.

3.5. Conclusion

This chapter provided a thorough literature survey of concurrent dual-band power amplifiers and discussed the performance degradation in those PAs. It was found that traditional dual-band PAs and concurrent dual-band linear PAs experience significant efficiency and output power drops when operated in concurrent mode. The detailed mathematical derivations were

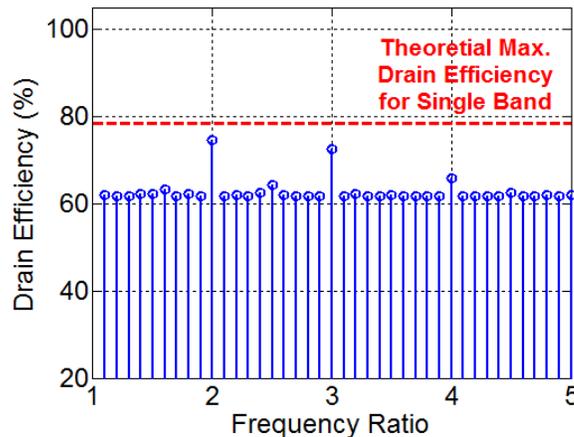


Fig. 3-8 Drain efficiency of the concurrent dual-band class-B PA as a function of frequency ratio

provided to show the mechanism of efficiency and output power drops in concurrent dual-band class-A and class-B PAs.

CHAPTER 4. CONCURRENT OPERATION IN SWITCH-MODE POWER AMPLIFIERS

4.1. Introduction

In Chapter 3 it was shown that concurrent dual-band linear PAs will have a significant efficiency and output power drop when working in concurrent mode compared to single mode or single-band counterparts. In [72], the authors tried to overdrive their concurrent dual-band PA for higher efficiency and output power, however the benefit of overdriving cannot be obtained with simply shorting harmonics and IMs to ground [24]. Traditionally in single-band PAs, switch-mode PAs are used to overcome the low efficiency of linear-mode PAs. For concurrent dual-band PAs, instead of a simple overdriving strategy, we turn to switch-mode PAs as a promising approach to improving the efficiency for concurrent dual-band PAs.

While the theoretical understanding and modeling of single-band switch-mode PAs is well understood, the application of this understanding does not directly lead to optimal designs for concurrent dual-band switch-mode PAs. So far, there is no effort has been made to explore the possible high efficiency of concurrent dual-band switch-mode PAs. In this chapter, a concurrent dual-band class-D power amplifier will be developed, through fundamental theory development, with practical design considerations, to actual PA implementation, and finally to measurement validation. As expected, the concurrent dual-band class-D PA did show superior drain efficiency and output power in concurrent mode than concurrent dual-band linear PAs did. A 100%

theoretical drain efficiency can be achieved, with lower than 1 dB output power drop compared to a 3 dB drop in linear concurrent dual-band PAs

The demonstration will be carried out through a current-switching class-D (CSCD) topology. The ideal assumption of the class-D PA used in Chapter 2 will be less accurate in a concurrent dual-band operation. In a single-band class-D PA, the transistors are treated as ideal switches with zero transition time and a constant finite knee voltage [25-29, 41]. In a concurrent dual-band class-D PA, on the other hand, transistors can no longer be treated as ideal switches. An ideal-switching assumption is only valid when the transistors are well overdriven. A concurrent dual-band signal, however, has a time varying envelope and cannot always overdrive the transistors. Under such circumstances, the DC current won't be fully switched to any of the transistors as is the case in a single-band class-D PA.

The assumption of constant knee voltage used in Chapter 2 also becomes inaccurate in concurrent operation. With a time-varying envelope of input signal, the on-resistance is also varying over time and thus should be considered as a function of gate-source voltage instead of a constant values as commonly treated in single-band class-D PA. The varying on resistance leads to a varying knee voltage. Detailed analysis regarding the transistor model and non-constant on-resistance will be presented in Section 4.2.

In addition to theoretical analysis, some practical consideration will also be resented in this chapter. A discussion of gate-bias impact on drain efficiency will be included in Section 4.4, which is important in both single-band and concurrent dual-band CSCD PAs. Actual harmonic and intermodulation terminations required by concurrent dual-band CSCD PAs are discussed in Section 4.5 where tradeoffs between single-mode and concurrent-mode performance will also be

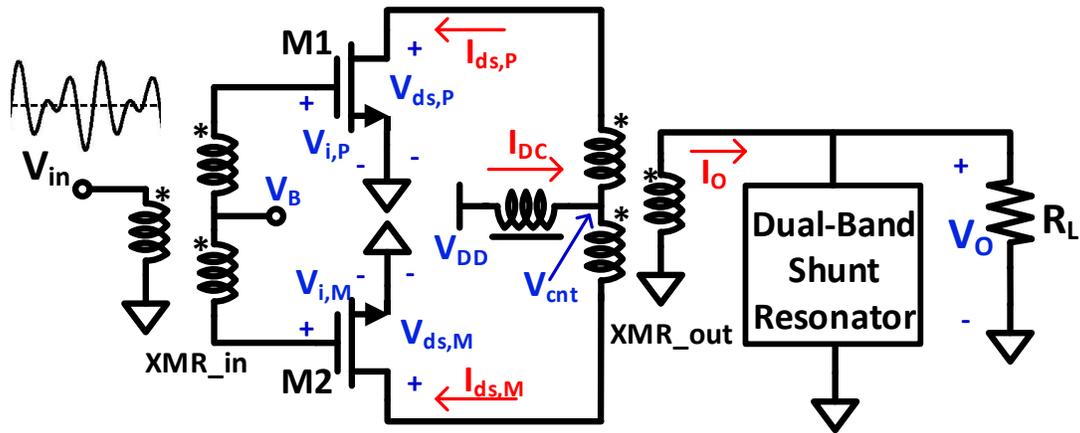


Fig. 4-1 Schematic of a push-pull current-switching class-D (CSCD) PA

discussed. The required termination profile indicates that CSCD PA becomes an inverse class F PA in GHz region as ideal termination for harmonics/inter-modulation components start to fall apart and only finite number of termination can be realized [24, 26-28]. Actual implementation of proposed concurrent dual-band class-D PA and measurement results will be presented in the next chapter.

4.2. Mathematical Model for a Concurrent Dual-Band Current-Switching Class-D Power Amplifier

The schematic of a concurrent dual-band current-switching class-D PA is quite similar to its single-band counterpart as shown in Fig. 4-1, except for the output shunt resonator. In a concurrent dual-band PA, a dual-band shunt resonator is required instead of a single-band resonator. Throughout this analysis, the optimal load impedance, R_L , is assumed to be resistive and is ready to be used. As in the analysis of concurrent dual-band linear type PAs in Chapter 3, the optimal load impedance is assumed to be the same for both frequency bands. For simplicity, the impedance matching network is not shown in this theoretical analysis; it will be discussed in the next chapter.

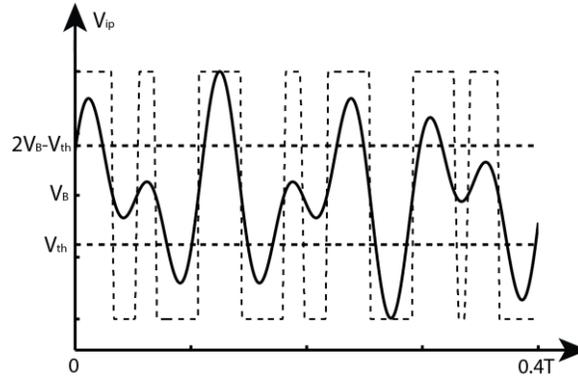


Fig. 4-2 Concurrent dual-band input signal (top transistor)

It was pointed out in the introduction that the ideal switch model and constant knee voltage are not valid for a concurrent dual-band class-D operation. As such, an accurate mathematical model must be developed before further analysis can commence. Our proposed model is based on the schematic of a push-pull current-switching class-D PA, shown in Fig. 4-1, where a dual-band shunt resonator is required instead of single-band shunt resonator in a single-band CSCD PA

A concurrent dual-band input signal split evenly into a pair of differential signals through an ideal transformer is expressed in the following:

$$V_{I,P}(t) = A_L \sin(\omega_L t) + A_H \sin(\omega_H t) + V_B \quad (4-1)$$

$$V_{I,M}(t) = A_L \sin(\omega_L t + \pi) + A_H \sin(\omega_H t + \pi) + V_B \quad (4-2)$$

where A_L and ω_L are the amplitude and angular frequency of the low-band signal, respectively, A_H and ω_H are the amplitude and angular frequency of the high-band signal, respectively, and V_B is the gate bias voltage. Notice that even though the low- and high-band signals, individually, have a constant envelope, the composite signals of (4-1) and (4-2) will have a time-varying envelope, as shown in Fig. 4-2. The input signal of a single-band class-D PA can be easily amplified and

approaches a square-like waveform [25]. In a concurrent dual-band case, however, it is almost impossible to obtain a square-like shape (the dashed lines in Fig. 4-2), as it may need impractical amplification and require a lot of higher-order harmonic/IM components which are very hard to obtain in GHz range. The result is that there will be significant portions of time during which both transistors, $M1$ and $M2$, are conducting current. Consequently, the DC current will not always be fully switched from one transistor to the next, and for a portion of each period, the DC current will

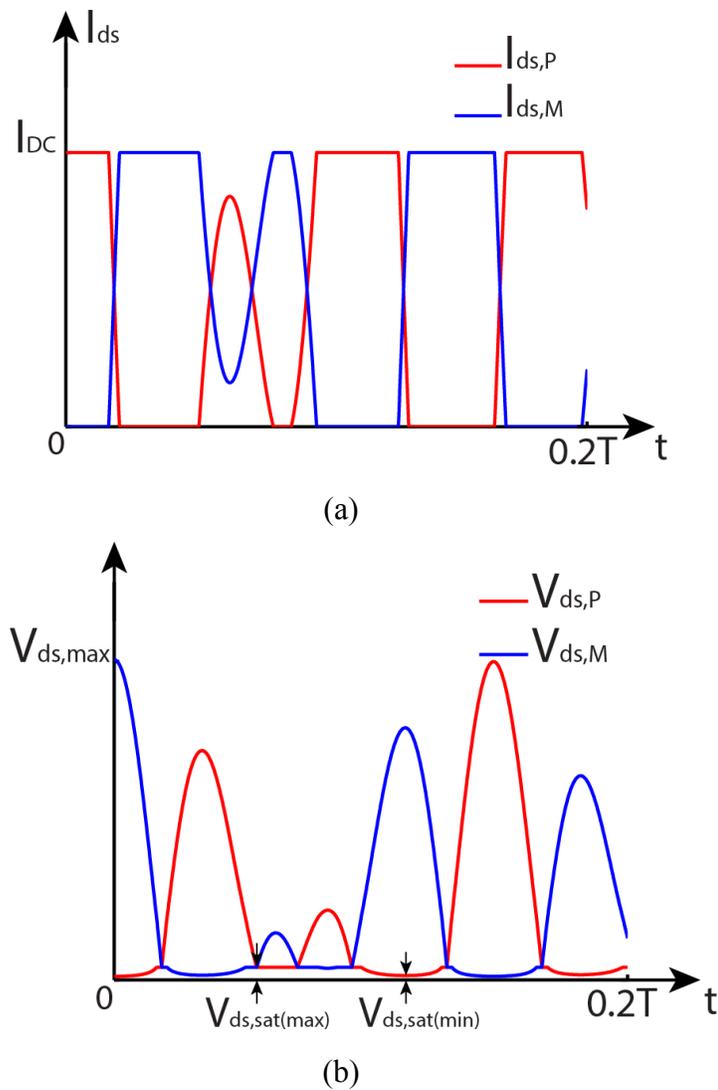


Fig. 4-3 Drain current waveform (b) Drain voltage waveform

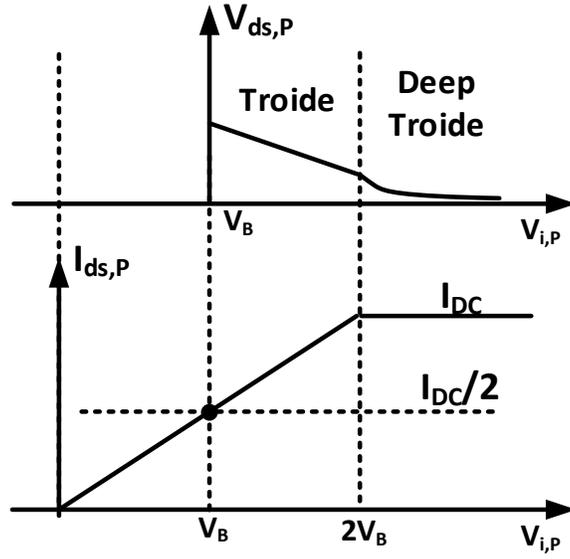


Fig. 4-4 Piece-wise linear behavior of transconductance

be split between the two transistors. Therefore, as seen in Fig. 4-3(b), the concurrent dual-band drain current cannot necessarily be described by a square wave. This is in direct contrast to the traditional single-band class-D PA where the DC current is fully switched from one transistor to the other, resulting in a near-square drain current waveform [25].

This behavior is modeled using a piece-wise linear equation for the drain current:

$$I_{ds,P(M)}(t) = \begin{cases} 0, & V_{i,P(M)} \leq V_{th} \\ \frac{I_{DC}}{2V_B} V_{i,P(M)}, & V_{th} < V_{i,P(M)} < 2V_B \\ I_{DC}, & V_{i,P(M)} \geq 2V_B \end{cases} \quad (4-3)$$

Equation (4-3) is shown graphically in Fig. 4-4, where it is assumed that $V_{th} = 0$. The value of I_{DC} is predefined, as is usually done in current-switching class-D or class-F-1 PA analyses [24-26, 32, 41, 42]. With the predefined I_{DC} , the DC supply in this analysis is left unfixed and will be calculated according to drain voltage. With the expressions of differential input signals in (4-1),

(4-2), and the model of transconductance in (4-3), drain current $I_{DSP(M)}$ then can be obtained simply by putting (4-1) and (4-2) into (4-3), resulting in a pair of differential drain current waveforms as shown in Fig. 4-3(a). Compared to the single-band case, the concurrent dual-band drain current waveform contains more portions when both transistors are conducting currents as expected.

Because the transistor cannot be modeled as an ideal switch under concurrent dual-band operation, it is necessary to re-examine the assumptions for $V_{ds,sat}$. In traditional single-band class-D PAs, a fixed current, I_{DC} , is assumed to switch between two transistors instantaneously. In other words, transistors are operating in a deep triode region in most of the time when they are on, as shown in Fig. 4-4. The drain-source saturation voltage, $V_{ds,sat}$, in this region is small and relatively constant. Thus, the assumption of a constant $V_{ds,sat}$ in the single-band class-D PA analysis is accurate. The behavior of $V_{ds,sat}$ under concurrent dual-band behavior is a bit more complicated, however, due to the non-complete switching of the transistors that occurs. The non-complete switching behavior causes the transistors to operate in the triode region which results in a larger

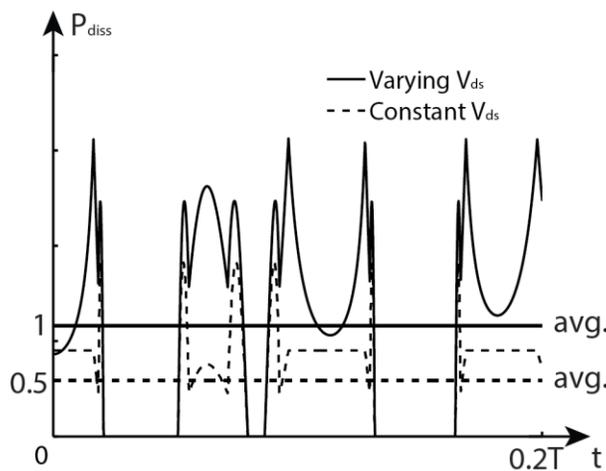


Fig. 4-5 Transistor power dissipation

$V_{ds,sat}$, as shown in Fig. 4-3(b). When the transistors are fully switched and enter the deep triode region, $V_{ds,sat}$ becomes small again. This variation in $V_{ds,sat}$ will increase power dissipation in transistors significantly. Fig. 4-5 plots the power dissipation in the transistors of the proposed concurrent dual-band current-switching PA under two scenarios: varying $V_{ds,sat}$ (solid line) and constant $V_{ds,sat}$ at $V_{ds,sat(min)}$. An increase by about a factor of 2 in power dissipation is observed with the varying $V_{ds,sat}$, which indicates that the simple assumption of a constant $V_{ds,sat}$ is no longer accurate in concurrent dual-band class-D PAs.

We capture the time-varying nature of $V_{ds,sat}$ by making the on-resistance of the transistor dependent on the gate voltage:

$$r_{on}(V_I) = \frac{1}{\kappa_p(|V_{I,P(M)} - V_B| + V_B)} \quad (4-4)$$

where κ_p is the transconductance parameters of the transistor. Notice that (4-4) is simply the expression for the channel resistance of a triode-region MOSFET. Now $V_{ds,sat}$ can be defined as:

$$V_{ds,sat} = I_{ds,P(M)} \cdot r_{on}(V_I) \quad (4-5)$$

It is assumed in (4-5) that $I_{ds,P(M)} > I_{DC}/2$ and $V_{I,P(M)} > V_B$, implying that $V_{ds,sat}$ is calculated when either transistor is driven above the bias point [25].

4.3. Maximum Drain Efficiency and Output Power

Using the previously described model, we now derive an expression for the maximum theoretical drain efficiency of a concurrent dual-band class-D PA. Generically, the drain efficiency is defined as:

$$\eta = \frac{P_{out}}{P_{DC}} \quad (4-6)$$

where P_{out} is the total power dissipated in the load resistance at ω_L and ω_H , and P_{DC} is the total power supplied from the DC supply.

To find an expression for P_{out} , we first recognize that the output current (I_0), in Fig. 4-1, can be expressed as:

$$I_0(t) = (I_{ds,P}(t) - I_{ds,M}(t)) / 2 \quad (4-7)$$

where it is assumed that the output transformer, XMR_{out} , has a transformation ratio of 1:1. Due to the nonlinear distortion of the switches, the output current contains both harmonic and intermodulation (IM) components which can be represented by expanding (4-7) using a Fourier series expansion:

$$I_0(t) \approx \sum_{n=0}^N \sum_{m=0}^M I_{(m,n)} \sin((m\omega_L \pm n\omega_H)t + \theta_{(m,n)}) \quad (4-8)$$

where m and n are used to index the frequency components (e.g., the fundamentals, IM, harmonics, etc.) of the output current. Assuming that the dual-band shunt resonator ideally removes all unwanted frequency components, only the fundamental components of the output current, $I_{(1,0)}$ and $I_{(0,1)}$, flow into the load resistance, R_L . The output power is therefore expressed as:

$$P_{out} = \frac{I_{(1,0)}^2 + I_{(0,1)}^2}{2} R_L \quad (4-9)$$

To find an expression for P_{DC} , we recognize that the output voltage is given as:

$$V_0(t) = R_L I_{(1,0)} \sin(\omega_L t + \theta_{(1,0)}) + R_L I_{(0,1)} \sin(\omega_H t + \theta_{(0,1)}) \quad (4-10)$$

which is reflected across the output transformer, XMR_{out} , and is dropped across M_1 and M_2 as $V_{ds,P}$ and $V_{ds,M}$. Similar to the single-band case, $V_{ds,P(M)}$ is defined as the summation of $V_{ds,sat}$ and the positive half cycle of the output voltage, V_0 , when the transistor is switched off [25]. We can now express the drain-source voltages as.

$$V_{ds,P}(t) = \left(\left| I_{ds,P}(t) - \frac{I_{DC}}{2} \right| + \frac{I_{DC}}{2} \right) r_{on}(t) + \frac{|V_0| + V_0}{2} \quad (4-11)$$

$$V_{ds,M}(t) = \left(\left| I_{ds,M}(t) - \frac{I_{DC}}{2} \right| + \frac{I_{DC}}{2} \right) r_{on}(t) + \frac{|V_0| - V_0}{2} \quad (4-12)$$

With $V_{ds,P(M)}$ defined, the DC supply voltage can now be expressed as:

$$V_{DD} = \frac{1}{T} \int_0^T V_{cnt}(t) dt = \frac{1}{2T} \int_0^T (V_{ds,P}(t) + V_{ds,M}(t)) dt \quad (4-13)$$

where T is so-called beat period of the dual-band input defined in (4-1) and (4-2). The beat period is given as the least common multiple of $1/f_L$ and $1/f_H$. Using (4-6), (4-9), and (4-13), the drain efficiency of the concurrent dual-band class-D PA can be expressed as:

$$\eta = \frac{(I_{(0,1)}^2 + I_{(1,0)}^2) R_L}{2V_{DD} I_{DC}} \quad (4-14)$$

Drain efficiency and output power are calculated numerically, assuming I_{DC} is 1 A, R_L is 1 Ω , ω_H/ω_L is 1.7, V_B is normalized to 1 V, and r_{on} (at $V_{i,P(M)} = V_B$) is normalized to 1/30 of R_L . As will be shown in the subsection below, the bias condition has considerable impact on the drain efficiency of a concurrent dual-band current-switching class-D or inverse class-F PA, which has never been rigorously explained before but was empirically picked in class-AB [32, 42, 75, 76].

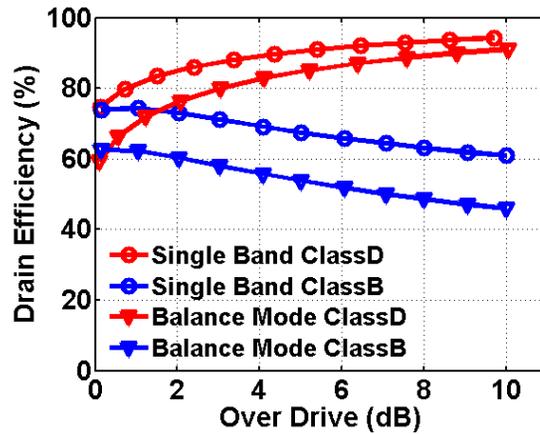


Fig. 4-6 Drain efficiency for ideal class-B and proposed class-D in single and concurrent dual-band modes

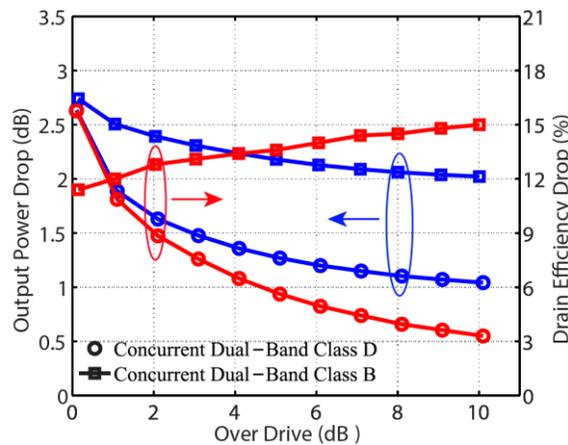


Fig. 4-7 Drain efficiency and output power reduction in concurrent dual-band class-B and class-D

The frequency ratio of ω_H/ω_L could be any value theoretically except for harmonic-related ratios (2, 3, etc.), but it is suggested that the ratio should be chosen such that their significant IM components (2nd and 3rd order) are not too close to the carrier frequencies for easy filtering purposes in actual design. The amplitude ratio could also be arbitrary within $(-\infty \sim +\infty)$, which covers a single-mode operation where either A_L or A_H is equal to zero and a balanced concurrent-mode operation where $A_L = A_H$, which is used in this example. Fig. 4-6 shows the balanced concurrent-mode drain efficiency as a function of overdrive level in both single mode and

concurrent mode. As a comparison, the drain efficiency of class-B PA is also plotted. From Fig. 4-6, it can be concluded that the proposed concurrent dual-band class-D PA provides very close to single-mode drain efficiency in concurrent mode as the PA is driven into deeper saturation. As an example, at 6dB overdrive level, the single-mode drain efficiency is around 92% while the concurrent-mode drain efficiency reaches 87%, which is only 5% lower. Class B, on the other hand, doesn't benefit from overdrive; the concurrent-mode drain efficiency is still 12-15% lower than single-mode case (a 16% drop would be observed with an ideal transistor [72, 74]). In fact, it has a lower drain efficiency as the PA is overdriven in concurrent mode, as well as in single mode [24]. The comparison demonstrates that, as in a single-band PA, a linear-mode PA in a concurrent dual-band operation also have an efficiency limit (61% in the example of class-B configuration) and one cannot improve the efficiency by simply overdriving it without any load re-termination. A switch-mode PA, however, still has the ability to obtain high efficiency in a concurrent dual-band operation, with minimum drop from its single-band counterpart, as it is driven into saturation.

Output power degradation in both concurrent dual-band class-B and the proposed class-D are plotted in Fig. 4-7. It can be seen that the proposed concurrent dual-band class-D PA has less output power reduction from its single-mode case than the concurrent dual-band class-B configuration under the same overdrive level. Fig. 4-6 and Fig. 7 show that the proposed concurrent dual-band class-D PA has the ability to achieve concurrent-mode efficiency and output power comparable to its single-mode counterpart.

4.4. Effects of Gate Bias on Efficiency

Bias effect on efficiency was seldom mentioned in class-D PA design due to its switching assumption, and was rarely discussed rigorously in class-F/F-1 PAs [32, 42, 75, 76] where bias is

usually empirically picked in class AB region. This sometimes led to misleading results [42, 76] that class F-1 or current-switching class-D PAs can be biased in the deep class-AB or class-B region. The following analysis will show that the bias for class-F-1 or current-switching class-D PAs should be biased above $I_{DC}/2$ so that in overdriven operation, as mentioned in previous subsections, both transistors will be in the triode region when $V_{iP}(t) = V_{iM}(t) = V_B$. Such a bias condition is defined as "bias in triode" in this thesis. As bias gets into the saturation region (DC bias current falls below $I_{DC}/2$), drain efficiency drops rapidly. Fig. 4-8 shows plots of the concurrent-mode drain efficiency as a function of gate bias under different load terminations. These plots were obtained by ADS simulation using transistor models with finite on resistance. The color curves are current-switching class-D PA terminations, with the green curve representing ideal termination (infinite harmonics/IM components), the red curve representing terminations up to 5th-order harmonics/IM components, and the blue curve representing terminations up to 3rd-order harmonics/IM components. The black curve, on the other hand, is class-B termination where all harmonics and IM components are shorted. So, Fig. 4-8 indicates that gate bias has a significant effect on drain efficiency in a concurrent dual-band class-D PA (color curve). Drain efficiency drops rapidly as gate bias gets farther from the optimal point. The cause of gate-bias effect comes from the finite channel resistance or output resistance, which is a function of gate voltage or overdrive voltage, as well as the operation region of the transistor. An AC load line depicted in Fig. 4-9 is used here to illustrate such a bias effect. Waveforms of drain currents and voltages under two different gate bias conditions are plotted on the same I-V figure, where the red line shows the bias-in-triode condition while the blue curve is the bias-in-saturation condition. If the transistors are biased in triode region as shown by the red curve in Fig. 4-9, V_{ds} is very small when $V_{iP}(t) = V_{iM}(t) = V_B$ because of a small on resistance in the triode region. The overall non-zero

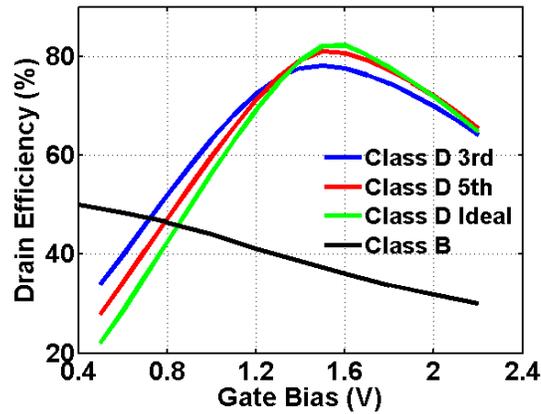


Fig. 4-8 Balanced concurrent-mode drain efficiency of proposed class-D PA as a function of bias

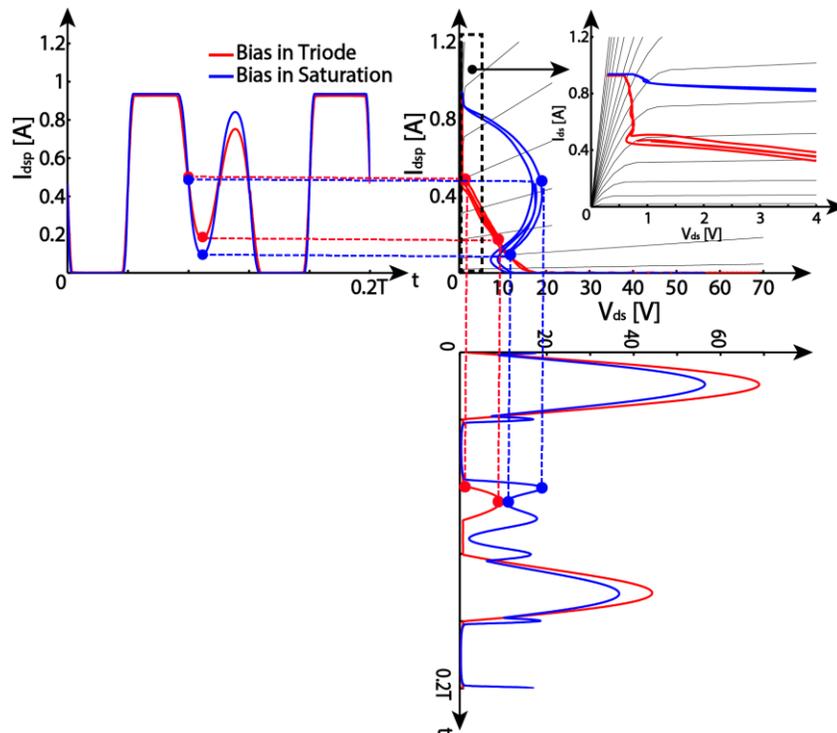


Fig. 4-9 Loadline of proposed class D PA bias in triode and saturation region overlap between drain current and voltage, or the area below the load line, is thus minimized. The case where transistors are biased in saturation region (blue line), however, has much more overlap and thus more power dissipation in the transistors. When the transistors are biased in saturation region, a large peak is generated in drain voltage at $V_{iP}(t) = V_{iM}(t) = V_B$ due large output

resistance causing a large non-zero overlap with the drain current in the vicinity of this point. The lower the gate bias is (under the same I_{DC}), the higher the drain voltage peak will be and thus there is more loss in transistors and lower drain efficiency. The above described current and voltage waveforms are based on the facts of short load impedance for odd-order harmonics/IM components and open load impedance for even-order harmonics/IM components. As the load termination becomes less ideal, the gate bias effect will become less significant, which is verified in Fig. 4-8 from the green curve to the blue curve. More uncontrolled harmonic/IM impedance leads to class B termination and the class-D PA no longer has the above gate bias effect. The slight efficiency roll-off when gate bias is above the optimal point is out of the scope of this thesis and not explained here.

4.5. Harmonic and Intermodulation Terminations

The above analysis described the behavior of an ideal concurrent dual-band current-switching class-D PA in concurrent mode, where an ideal load network with an ideal transformer were assumed. While we were able to calculate efficiency and output power numerically, there was no information provided as to how the load network should be designed. The following analysis will provide insights on how different frequency components should be properly terminated in the load network by deriving the frequency components contained in drain current and voltage.

To find the frequency components in the drain current, the piece-wise linear model for transconductance in (4-3) can be first expanded into polynomials and then put input signals (4-1) (4-2) into the polynomials. To obtain the polynomial approximation of (4-3), which is also depicted in Fig. 4-4, we first approximate a simpler and more familiar curve (shown in Fig. 4-10),

which can then scale and shift to obtain the expression for (4-3). It is symmetric around the origin and thus can be expressed using only odd-order powers.

$$f(x) \approx x_0 + \sum_{n=1}^N \alpha_{2n-1} x^{2n-1} \quad (4-15)$$

where x_0 is the DC offset and the coefficients α_{2n-1} control the saturation point, v_{sat} . The above polynomial expression is valid within the interval of $[-1, 1]$. The saturation point is arbitrary as long as the clip area ($[v_{sat}, 1]$ and $[-1, -v_{sat}]$) is large enough to include the investigated overdrive level. For example, an overdrive of 20 dB can be covered when v_{sat} is equal to 0.1. Now, let

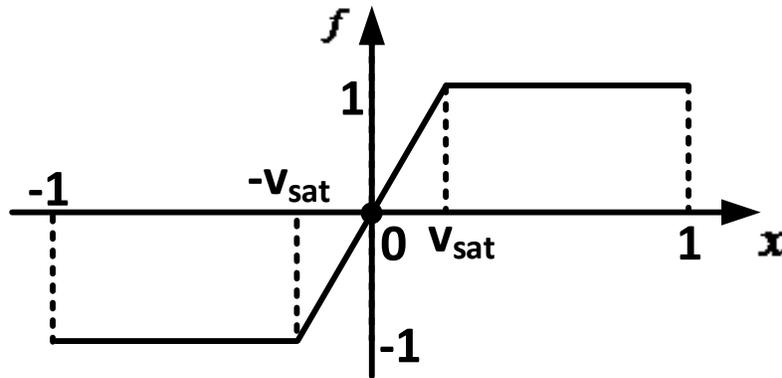


Fig. 4-10 Template function for power series expansion of the drain current

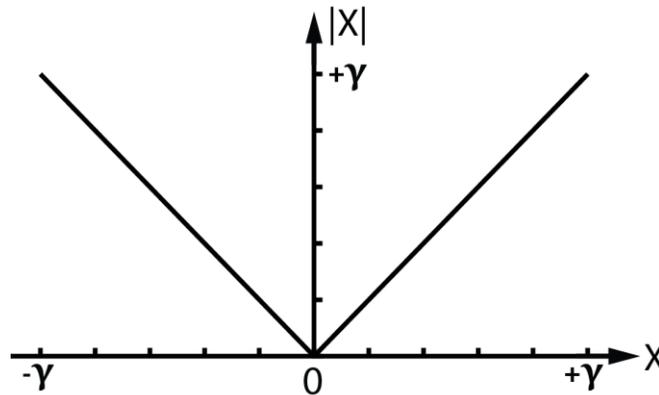


Fig. 4-11 Power series approximation of the absolute value function

$f(x) = I_{ds,P(M)}$ and $x = V_{i,P(M)}$. The Taylor series of the drain current defined in (4-3) can be obtained by shifting and scaling (4-15):

$$I_{ds,P(M)}(V_{i,P(M)}) \approx \frac{I_{DC}}{2} + \frac{I_{DC}}{2} \cdot \left(\sum_{n=1}^N \alpha_{2n-1} \left(\frac{V_{i,P(M)}}{\rho V_B} - \frac{\rho v_{sat}}{\rho} \right)^{2n-1} \right)$$

$$= \begin{cases} \sum_{k=0}^K \sum_{j=-J}^J I_{ds,P(k,j)} * \sin \left((k\omega_2 + j\omega_1)t + \theta_{ds,P(k,j)} \right) \\ \sum_{k=0}^K \sum_{j=-J}^J I_{ds,M(k,j)} * \sin \left((k\omega_2 + j\omega_1)t + \theta_{ds,M(k,j)} \right) \end{cases}, \quad (4-16)$$

where the coefficient, ρ , is chosen such that $\rho/\rho v_{sat}$ is greater than the desired overdrive level. There is a trade-off between accommodating larger overdrive levels and increasing N in order to maintain an accurate approximation. Expression (4-16) shifts (4-15) by a vector of $(v_{sat}, 1)$. It also scales (4-15) by ρV_B on the x axis and $I_{DC}/2$ on the y axis. Since the power series in (4-16) contains only DC and odd power, it can be expected that the frequency components in the drain current are all odd-order harmonics and inter-modulation components other than fundamentals and DC components; in other words, $(k + j)$ is equal to an odd number.

To expand the drain voltage expressed in (4-11) and (4-12) requires the previously derived polynomial expansion of the drain current, as well as the polynomial expansion of the absolute value function. The absolute value function, plotted in Fig. 4-11 over the interval of $x = [-\gamma, +\gamma]$, can be expressed as:

$$f_v(x) \approx \beta_0 + \gamma \sum_{m=1}^M \beta_{2m} (x/\gamma)^{2m} \quad (4-17)$$

where γ is chosen to be large enough to accommodate the required values for $V_{i,P(M)}$, $I_{ds,P(M)}$, and V_0 . Larger values for γ will support larger drain voltages, but at the expense of increased values

for M . The DC component, β_0 , is kept small enough to be approximately equal to zero and is neglected in the following equations. In this thesis, the γ should be above 80 because the maximum value for x in (4-17) is the peak value of the output voltage (V_o) and would be as large as 80V due to the high breakdown voltage of GaN transistors. Applying (4-17) and (4-16) into (4-11) and (4-12), the Taylor series of drain voltage can be obtained:

$$\begin{aligned}
 V_{ds,P(M)}(t) &= \left(\left| I_{ds,P(M)}(t) - \frac{I_{DC}}{2} \right| + \frac{I_{DC}}{2} \right) * r_{on}(t) + \frac{|V_o(t)| \pm V_o(t)}{2} \\
 &= \frac{a + I_{DC}/2}{k_p(b + V_B)} + \frac{1}{2}(c \pm V_o) \\
 &= \begin{cases} \sum_{p=0}^P \sum_{q=-Q}^Q V_{ds,P(p,q)} * \sin((p\omega_2 + q\omega_1)t + \theta_{ds,P(p,q)}) \\ \sum_{p=0}^P \sum_{q=-Q}^Q V_{ds,M(p,q)} * \sin((p\omega_2 + q\omega_1)t + \theta_{ds,M(p,q)}) \end{cases} \quad (4-18)
 \end{aligned}$$

where k_p is defined in (4-4), V_o is defined in (10), and

$$a = \left| I_{ds,P(M)} - \frac{I_{DC}}{2} \right| \approx \gamma \sum_{m=1}^M \beta_{2m} \left(\frac{I_{ds,P(M)}}{\gamma} - \frac{I_{DC}}{2\gamma} \right)^{2m}, \quad (4-19)$$

$$b = |V_{i,P(M)} - V_B| \approx \gamma \sum_{m=1}^M \beta_{2m} \left(\frac{V_{i,P(M)} - V_B}{\gamma} \right)^{2m}, \quad (4-20)$$

$$c = |V_o| \approx \gamma \sum_{m=1}^M \beta_{2m} (V_o/\gamma)^{2m}, \quad (4-21)$$

In (4-18), $I_{ds,P(M)}(t)$ contains fundamentals and odd-order harmonics/IM components as shown in (4-16), while $V_o(t)$ and $V_{IP(M)}(t)$ contains only fundamentals. We thus can expect that only even-order frequency components are contained in drain voltage (other than fundamentals and DC components), since the absolute function approximation has only even-order power series, as shown in (4-17). A rigorous expression of magnitude can be calculated for each frequency

component; however for simplicity and intuition, numerical calculation is used here. By finding the coefficients for (4-15) and (4-17), and using the same assumption for I_{DC} , R_L , the frequency ratio, k_p and V_B , as in section 4.3, the results of the frequency components in drain current and voltage, up to 5th order, are obtained and shown in Table 4-1.

4.5.1. Ideal Termination

From (4-16) and (4-18), we know that an infinite number of polynomials are needed to build the drain current and voltage shown in Fig. 4-3(a) and (b). Since drain current contains only odd-order harmonics and inter-modulation components, while drain voltage has only even-order harmonics and inter-modulation components, the load network must provide a short circuit for odd-order harmonics and inter-modulation components and an open circuit for even-order harmonics and inter-modulation components. Ideally, the load network shown in Fig. 4-1 covers an infinite number of harmonic and IM terminations. Such an ideal load termination provides the

Table 4-1 Magnitude of the different frequency components presented in drain current and drain voltage

Frequency Component	Order of Nonlinearity	V_{ds}	I_{ds}	Frequency Component	Order of Nonlinearity	V_{ds}	I_{ds}
0	0	0.178	0.5	$2f_L-f_H$	3	0	0.123
f_L	1	0.197	0.4	$2f_H-f_L$		0	0.123
f_H		0.197	0.4	$2f_L+f_H$		0	0.123
f_H-f_L	2	0.101	0	$2f_H+f_L$	5	0	0.123
f_L+f_H		0.101	0	$3f_L$		0	0.025
$2f_L$		0.034	0	$3f_H$		0	0.025
$2f_H$		0.034	0	$3f_L-2f_H$		0	0.064
$2f_H-2f_L$	4	0.02	0	$3f_H-2f_L$	5	0	0.064
$2f_H+2f_L$		0.02	0	$3f_L+2f_H$		0	0.064
$3f_L-f_H$		0.0062	0	$3f_H+2f_L$		0	0.064
$3f_H-f_L$		0.0062	0	$4f_L-f_H$		0	0.005
$3f_L+f_H$		0.0062	0	$4f_H-f_L$		0	0.005
$3f_H+f_L$		0.0062	0	$4f_L+f_H$		0	0.005
$4f_L$		0.0012	0	$4f_H+f_L$		0	0.005
$4f_H$		0.0012	0	$5f_L$		0	0.005
			$5f_H$	0	0.005		

best performance in both single mode and concurrent mode. However, due to the parasitics of transistors and limited bandwidth of transformer/passive components, only a few frequency components can be properly terminated in real design. Most PAs cover only up to 3rd-order nonlinearities, with little performance gained when terminating beyond [30, 31, 37-39, 77]. The design of a practical load network for the proposed concurrent dual-band class-D PA becomes very difficult due to the large number of inter-modulation components. From Table 4-1, we can see that the inter-modulation components are much more important than harmonics. What frequencies need to be properly terminated thus becomes a critical and important task.

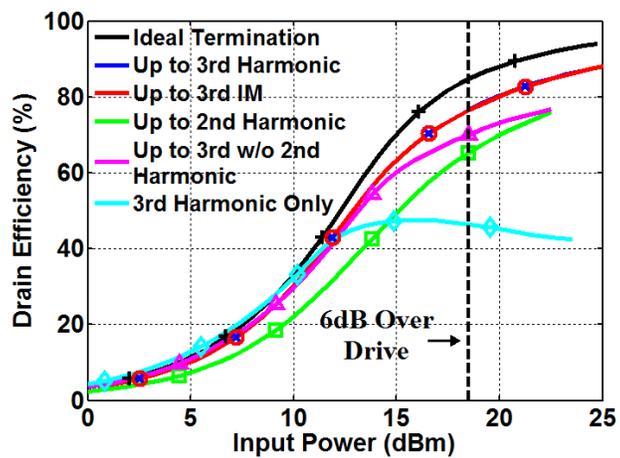
4.5.2. Finite Termination

The load termination requirement of the proposed concurrent dual-band class-D PA is the same as an inverse class-F configuration. In a single-band inverse class-F PA, 87% drain efficiency can be achieved if the load network is terminated up to the 3rd-order harmonics [30, 31, 78]. In the concurrent dual-band case, the same idea applies. A finite number of harmonic and IM terminations could result in good enough efficiency. However, the load terminations become much more complicated in the concurrent dual-band case, even when only up to the 3rd-order harmonics/IM components are considered. As shown in Table 4-1, there is a total number of 10 harmonics and IM components existing up to 3rd-order nonlinearity in the concurrent dual-band case, instead of two (2nd and 3rd harmonics) in the single-band case. To have a practical load network design, tradeoffs have to be made between efficiency and termination complexity. It can be observed from Table 4-1 that IM components plays more important roles in building up required waveforms than harmonics do. Thus, neglecting harmonics is expected to have a minimum drain efficiency drop. To evaluate the tradeoffs, ADS simulations were performed for both concurrent

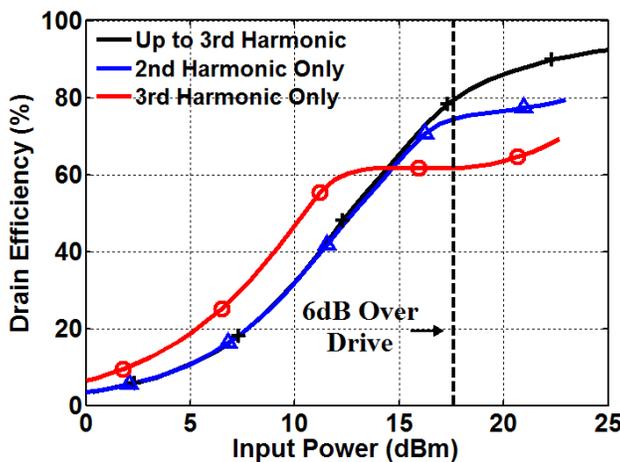
mode and single mode using actual transistor models and a numerical load tuner which could provide arbitrary impedance for an arbitrary number of frequencies. In concurrent mode, simulations were done under different configurations: 1) termination of all frequency components up to 3rd-order; 2) termination of components up to 3rd-order, neglecting 3rd-harmonics; 3) termination up to 2nd-order only, neglecting all 3rd-order terms; 4) termination up to 3rd-order, neglecting 2nd-harmonics; and 5) termination of only 3rd-order nonlinearities, neglecting all 2nd-order terms. The resulting drain efficiency, as a function of input power, is shown in Fig. 4-12(a), along with the ideal case where an infinite number of frequency components are terminated, for comparison.

It can be seen in Fig. 4-12(a) that controlling the termination impedance up to only the 3rd-order results in an 8% drop in drain efficiency from the ideal case at 6 dB of overdrive. This is deemed acceptable given the dramatic simplification in the load network. Moreover, it can be observed that neglecting 3rd-harmonics has little-to-no effect on drain efficiency. Additional simplification can be obtained by also neglecting 2nd-harmonics and IM3 components, resulting in a maximum drain efficiency of 70%. Neglecting IM2 components, on the other hand, results in a massive 30% reduction in drain efficiency. These results agree with Table 4-1, where it can be seen that the coefficients for the IM2 components are almost two orders of magnitude larger than either the IM3 or the 3rd-harmonics. The above results agree with the previous observation from Table 4-1 that IM components are much more important than harmonics, and indicate that 2nd-order IM components have to be terminated open, while 2nd-order harmonics and 3rd-order harmonics/IM components can be neglected if design complexity is a concern.

The above results only consider a concurrent dual-band operation. It is quite likely that a dual-band PA will be used in single-band operation, operating at ω_L or ω_H only. Therefore, the drain efficiency in a single-band operation should also be considered. For this, simulations were performed for several cases: 1) termination of all frequency components up to 3rd-order; 2) termination of all frequency components up to 2nd-order; and 3) termination for only 3rd-order nonlinearities, neglecting all 2nd-order terms. The results are shown in Fig. 12(b). Whereas correct termination of the 2nd-harmonic can be neglected in a concurrent dual-band operation, neglecting



(a)



(b)

Fig. 4-12 Drain efficiency under different termination (a) concurrent mode (b) single mode

the 2nd-harmonic in a single-band operation leads to a 20% drop in drain efficiency at 6 dB overdrive. However, an acceptable drain efficiency can still be obtained when correct termination of the 3rd-harmonic is neglected.

For maximum simplification of the load network and acceptable drain efficiency in both single-band and concurrent dual-band operations, we must control the termination impedance of the two fundamentals, the IM2 components and the 2nd-harmonic. Correct termination of the remaining frequency components can be neglected, but if increased area and design complexity can be tolerated, then correctly terminating the IM3 components will increase the drain efficiency by about 11%.

4.6. Conclusion

A concurrent dual-band current-switching class-D power amplifier is developed in this chapter. New behavioral and mathematical models are presented for the PAs and performance in terms of efficiency and output power are obtained, based on the new model. It was found that the proposed switch-mode PA can achieve comparable efficiency and output power than its single-band case. Some practical considerations are then discussed in order to guide actual design. For the proposed PA, it is necessary to control IM2 components and harmonics as they have a significant impact on efficiency. On the other hand, IM3 and harmonics are less important than IM2 and harmonics and could be traded off for easier design with an acceptable efficiency sacrifice.

CHAPTER 5. IMPLEMENTATION OF PROPOSED POWER AMPLIFIER AND MEASUREMENT RESULTS

5.1. Introduction

To prove the superior efficiency and output power of the proposed concurrent dual-band class-D PA analyzed in previous chapters, an actual power amplifier was implemented based on the harmonic and IM termination requirements discussed in Section 4.5. The termination profile includes open terminations for 2nd-order harmonics/IM components and short terminations for IM3 (neglecting 3rd-order harmonics). Optimal fundamental impedances are assumed the same and determined in a way to make the most of the transistors' power capacities. Power transistors used in the design are Cree's CGH40006P, which have a drain current rating of 0.75 A and drain-source voltage rating of 84 V. A I_{DC} of 0.5A is chosen to guarantee reliable operation of the transistors. Such I_{DC} will result in about a 0.2 A drain current in magnitude at each fundamental frequency in each transistor. A single-ended fundamental impedance of 100 Ω is then chosen, which results in a 20 V drain voltage in magnitude at each fundamental for each transistor. Considering the half-sinusoidal rectified nature of the drain voltage in the proposed PA, the peak value for such drain voltage is about 80V—below the transistor's voltage rating. The DC component, or average, of the drain voltage is about 18 V. Two frequencies for this design are 870 MHz and 1.49 GHz, which have a frequency ratio of 1.7 and are two bands for LTE. Based on above parameters, a detailed design of each part will be presented in this chapter followed with measurement results and discussion.

5.2. Realistic Load Impedance Profile

The load impedance requirements for fundamentals, harmonics, and IM components are the impedances seen by the intrinsic drain node from the transistor shown in Fig. 5-1, the actual load impedance ($Z_{L,actual}$) profile provided by the load network should de-embed the effect of the parasitic network from the transistor and package. Fortunately, the new transistor model from Cree provides access to the intrinsic drain node, allowing calculation of the total load impedance seen by the node. With this extra accessibility, the two-port Z-parameters of the output capacitor and package parasitic network are obtained by achieving an AC simulation on the schematic shown in Fig. 5-2. After obtaining the Z-parameters, the actual load impedance can be obtained by a simple S-parameter simulation as shown in Fig. 5-3 where the left-hand side of the Z-parameter symbol is terminated with an intrinsic load impedance profile (fundamental impedance is $100\ \Omega$ because Fig. 5-3 is single ended). Then, the impedance seen on the right-hand side is the conjugate of the

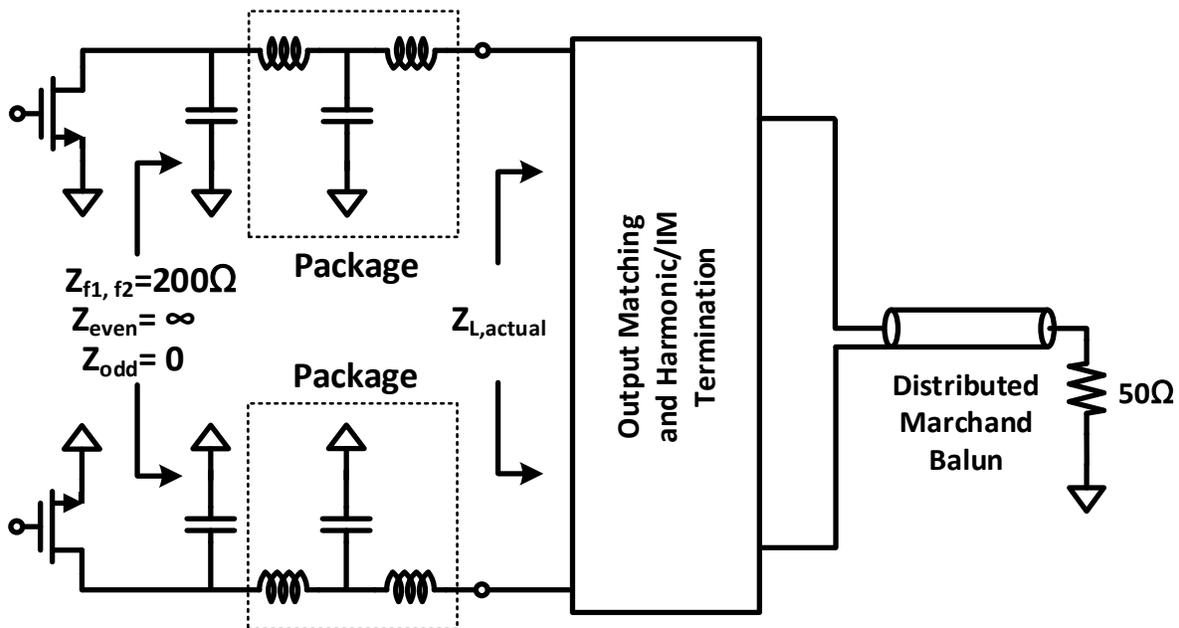


Fig. 5-1 Simplified package model of a GaN transistor

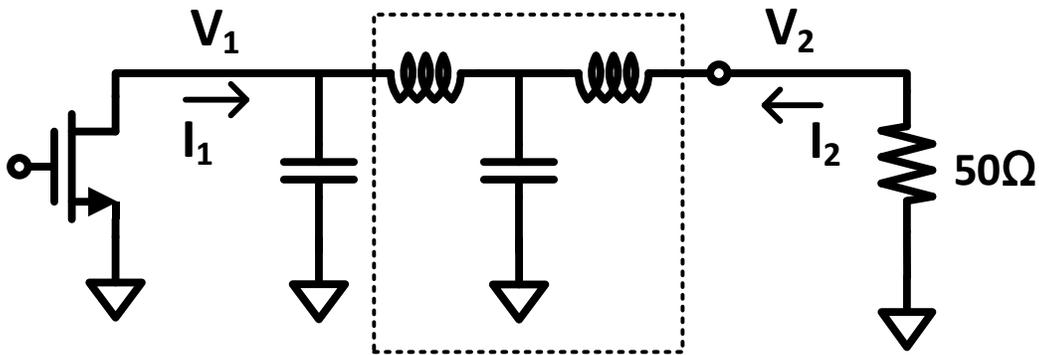


Fig. 5-2 Actual load impedance calculation

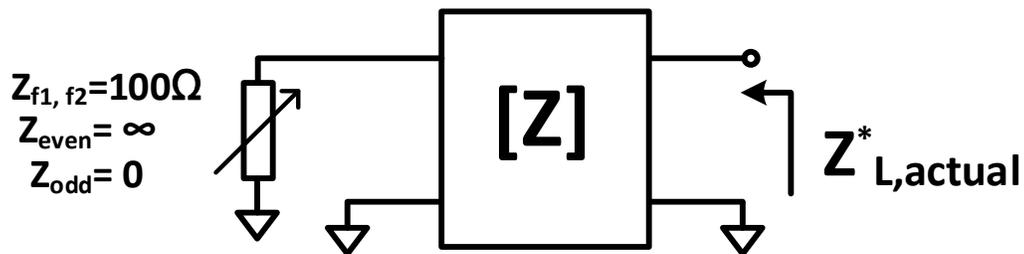


Fig. 5-3 Schematic for Z-Parameter simulation

actual load impedance, $Z_{L,actual}$. Note, the impedance obtained here is a single-ended value; the differential value should be doubled.

After de-embedding the transistor output capacitance and package parasitic network, the target load impedance profile is obtained and shown in Fig. 5-4. This profile assumes a non-foster behavior, which indicates a difficult, complex realization in a single-ended load network. A differential load network shown in Fig. 5-5 has an ability to mitigate design difficulties by separating termination for differential signals and common-mode signals, since the common-mode parts (in dashed boxes) are only seen by common-mode signals and are shorted to ground for differential signals. In the proposed push-pull PA, fundamental components and odd-order harmonics/IM components are differential signals (red dots in Fig. 5-4), while even-order harmonics/IM components are common-mode signals (blue dots in Fig. 5-4). The proposed

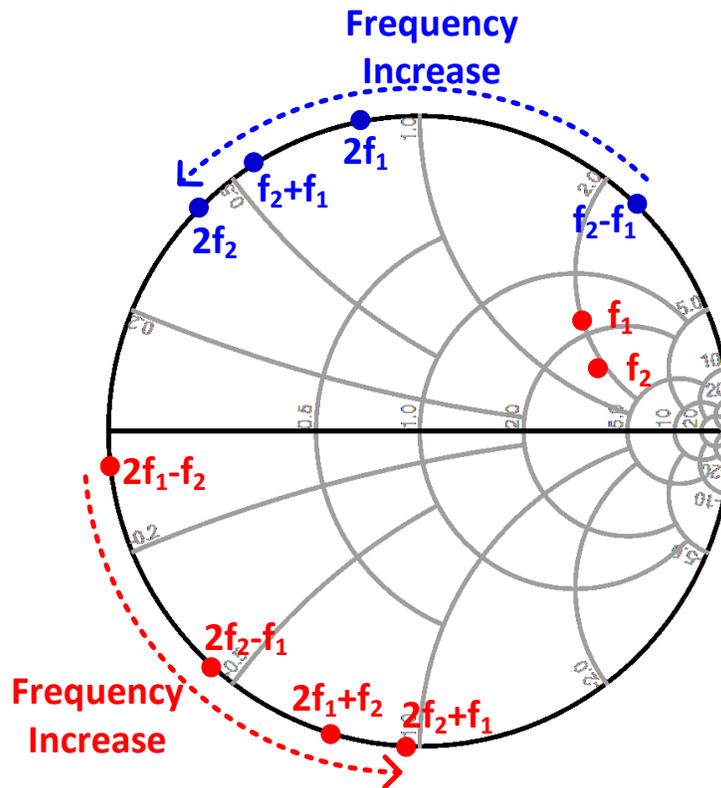


Fig. 5-4 Actual load impedance on the Smith Chart

differential network contains a single-layer output balun transformer, two matching sections A and B, and necessary feedline and inter-connections.

5.3. Broad-Band Marchand Balun

The target of the balun transformer is to provide a broadband balance-to-unbalance conversion as well as a 1:4 impedance transformation that matches 50Ω (single-ended port) to 200Ω seen at the differential ports. Since the substrate used in this design is a simple two-layer substrate, we need to use a coplanar structure for the balun transformer. A simplest coplanar balun is shown in Fig. 5-6—simply a pair of coupled line. Figure 5-6(a) shows the cross-section of the balun, while Fig. 5-6(b) presents the ideal model for the balun. Ideally, if the even-mode characteristic impedance of the coupled line (Z_{0e}) is infinite, then only a differential-mode signal

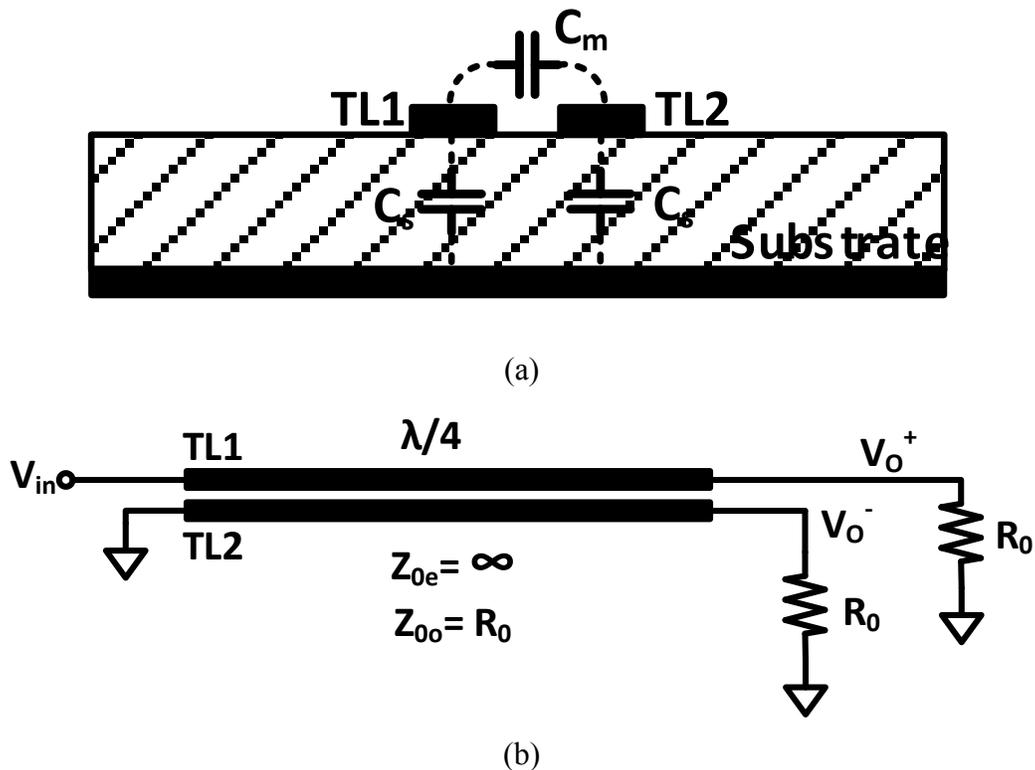


Fig. 5-6 Coupled-line balun (a) cross section (b) distributed model

Transformer

Fig. 5-5 Differential load network

propagates through the coupled line. An even-mode signal will have an open circuit for most cases except for half-wavelength. In such cases, the coupled line becomes an ideal balun with perfect magnitude/phase balance and infinite bandwidth when port terminations are matched to odd-mode characteristic impedance of the coupled line as shown in Fig. 5-6(b). Coaxial cables or twisted cables (sometimes with a toroid) provide good approximations to such ideal behavior [79-82]. In the case for the coplanar coupled-line balun shown in Fig. 5-6, the even-mode characteristic impedance of the coupled line (Z_{0e}) is not too much higher than the odd-mode characteristic impedance (Z_{0o}). Thus, significant even-mode components propagate within the coupled line. The even-mode characteristic impedance (Z_{0e}) becomes the characteristic impedance of each

transmission line (TL1 and TL2) reference the ground plane. These two transmission lines are regarded as parasitic transmission lines in the balun structure as shown in Fig. 5-7. Note, Z_o denotes the characteristic impedance resulting from the mutual coupling (C_m) of TL1 and TL2 excluding the characteristic impedance referenced to ground (C_s). The existing of the parasitic transmission line for TL1 (characterized with $Z_{o,inner}$) introduces another path to deliver power from the input port to the in-phase port at the output as shown in Fig. 5-8. This extra path causes the input power to unevenly split between the in-phase and out-of-phase ports at the output with more power delivered to the in-phase port. To equalize the output power between the two

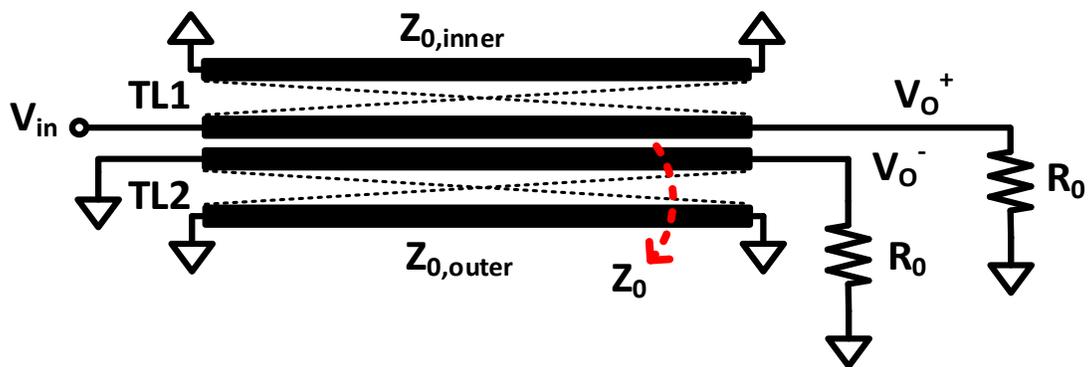


Fig. 5-7 Equivalent model of parasitic transmission line of the coupled-line balun

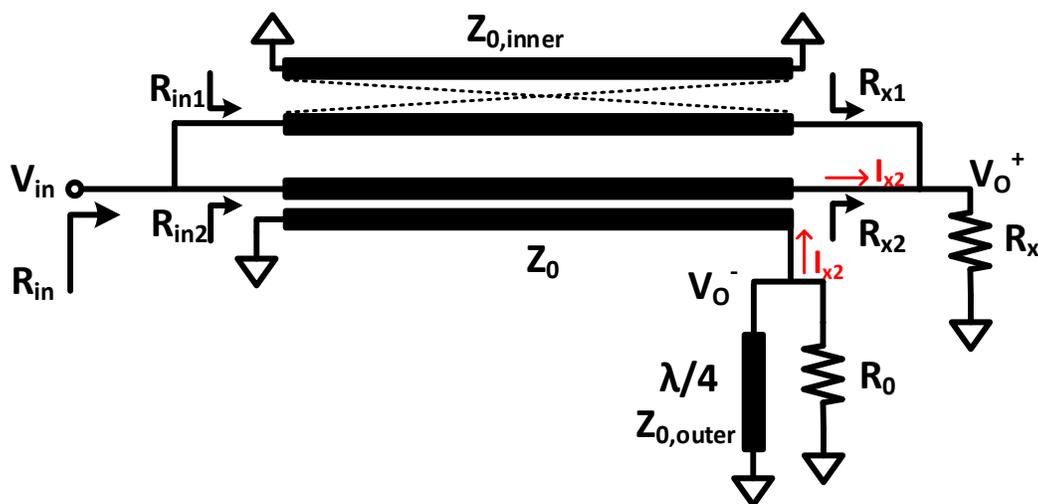


Fig. 5-8 Parasitic transmission-line of the coupled-line balun

differential ports, termination at the in-phase port should be reduced ($R_x < R_o$). The parasitic transmission line for TL1 (characterized with $Z_{o,outer}$), on the other hand, simply adds a shortened stub to the out-of-phase port in parallel (Fig. 5-8).

To realize the reduced termination, R_x , a transformer should be designed to transform standard termination, R_o , to R_x . The right-hand component of Fig. 5-9 shows such a circuit quite similar to the original coupled line to realize the impedance transformation. This added component is called a compensation stub characterized with Z_{stub} , $Z_{stub,inner}$, $Z_{stub,outer}$, respectively, Z_o , $Z_{o,inner}$, $Z_{o,outer}$. The balun structure shown in Fig. 5-9 is called a Marchand Balun [83]. Unfortunately, this seminal paper by Marchand is difficult to obtain and derived papers [84-87] do not provide a sufficient, detailed derivation and optimization of Marchand's original Balun structure. Therefore, a detailed mathematical derivation will be provided for the original Marchand Balun followed with optimization to achieve the best balance and widest bandwidth.

The reduced termination of the in-phase port at the output (R_x) is first derived at the electrical length of $\lambda/4$. To calculate R_x , first calculate the value of R_{1x} and R_{2x} as shown in Fig. 5-8. Assume the transmission lines are lossless. Then, the input power should be equal to the output power:

$$P_{in1} = P_{x1}, \quad (5-1a)$$

$$P_{in2} = P_{x2}, \quad (5-1b)$$

where:

$$P_{in1} = \frac{V_{in}^2}{2R_{in1}}, \quad (5-2a)$$

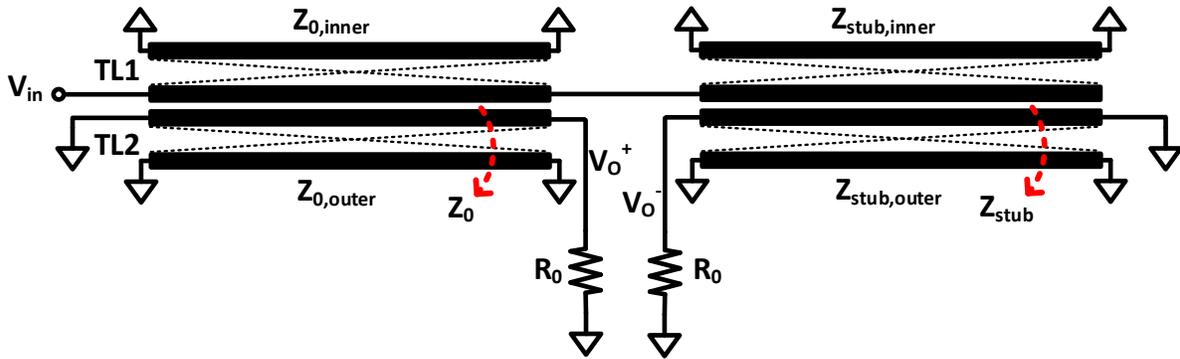


Fig. 5-9 Marchand balun – compensated coupled-line balun

$$P_{in2} = \frac{V_{in}^2}{2R_{in2}}, \quad (5-2b)$$

and

$$P_{x1} = \frac{V_o^{+2}}{2R_{x1}}, \quad (5-3a)$$

$$P_{x2} = 0.5 * \left(\frac{V_o^+}{R_{x2}}\right)^2 * (R_{x2} + R_o). \quad (5-3b)$$

From (5-1):

$$\frac{P_{in1}}{P_{in2}} = \frac{P_{x1}}{P_{x2}}. \quad (5-4)$$

When applying (5-2) and (5-3) into (5-4), the following relationship can be obtained:

$$\frac{R_{in2}}{R_{in1}} = \frac{R_{x2}^2 / (R_{x2} + R_o)}{R_{x1}}. \quad (5-5a)$$

R_{in1} and R_{in2} are converted from R_{x1} and $R_{x2} + R_o$ through their corresponding quarter-wavelength transmission line, respectively:

$$\frac{\frac{Z_o^2}{R_{x2}+R_o}}{\frac{Z_{o,inner}^2}{R_{x1}}} = \frac{R_{x2}^2/(R_{x2}+R_o)}{R_{x1}} \quad (5-5b)$$

Finally, the relation between R_{x1} and R_{x2} can be obtained:

$$\frac{Z_{o,inner}^2}{Z_o^2} = \frac{R_{x1}}{R_{x2}} = k^2, \quad (5-5c)$$

In (5-5), the total termination at the out-of-phase port is R_o since the shorted stub presents open circuit at electrical length of $\lambda/4$. Since R_x is simply the parallel combination of R_{x1} and R_{x2} , R_x is calculated as:

$$R_x = \frac{R_{x1}}{k+1} = \frac{kR_{x2}}{k+1} \quad (5-6)$$

Now, to ensure equal power split between the in-phase and out-of-phase ports, the following relation should be satisfied:

$$P_x = P_o, \quad (5-7a)$$

Expanding the expression for P_x and P_o using I_{x2} , (5-7a) becomes:

$$\frac{(R_{x2} \cdot I_{x2})^2}{2R_x} = \frac{(R_o \cdot I_{x2})^2}{2R_o}, \quad (5-7b)$$

Finally, the condition to maintain equal power split can be obtained:

$$\frac{R_x}{R_o} = \left(\frac{R_{x2}}{R_o} \right)^2. \quad (5-7c)$$

Applying the relation of R_x and R_{2x} in (5-6) into (5-7), we can obtain the reduced termination, R_x , with respect to R_o :

$$R_x = \left(\frac{k}{k+1}\right)^2 \cdot R_o \quad (5-8)$$

With the reduced termination R_x obtained, now calculate the input impedance, which is the parallel combination for R_{in1} and R_{in2} :

$$\begin{aligned} R_{in} &= R_{in1} \parallel R_{in2} \\ &= \frac{Z_{o,inner}^2}{R_{x1}} \parallel \frac{Z_o^2}{R_{x2} + R_o} \\ &= \frac{Z_o^2}{2R_o}. \end{aligned} \quad (5-9)$$

Equation (5-9) indicates a very interesting conclusion that the couple-line balun in Fig. 5-8 acts as an impedance transformer as well as a balun, as long as the reduced termination R_x fulfills the relationship in Eq. (5-8). Simply choose the necessary Z_o to realize the impedance transformation, 1:4, for example in this thesis, instead of using the multiple Marchand Balun section to realize impedance transformation [79-82]. And as will be determined later, the extra impedance transformation helps improve the bandwidth for the balun.

Next, derive the input impedance of the compensated stun as shown in Fig. 5-10. Since the electrical length is also $\lambda/4$, the input impedance for each path is expressed as:

$$R_{in1} = \frac{Z_{stub,inner}^2}{R_i}, \quad (5-10a)$$

$$R_{in2} = \frac{Z_{stub}^2}{-R_i} + R_o, \quad (5-10b)$$

where R_i is an impedance at the open end of the stub as shown in Fig. 5-10. Again, the stub is assumed to be lossless which lead to equal input and output power:

$$P_{in} = P_o, \quad (5-11a)$$

By expanding the expression for input and output power, (5-11 a) becomes:

$$\frac{V_{in}^2}{2R_{in1}} + \frac{V_{in}^2}{2R_{in2}} = \frac{(I_{in2} \cdot R_o)^2}{2R_o}, \quad (5-11b)$$

where $I_{in2} = V_{in}/R_{in2}$. The final result is:

$$\frac{1}{R_{in1}} + \frac{1}{R_{in2}} = \frac{R_o}{(R_{in2})^2}. \quad (5-11c)$$

Using Eqs. (5-10) and (5-11), obtain the relationship between R_{in1} , R_{in2} and R_o :

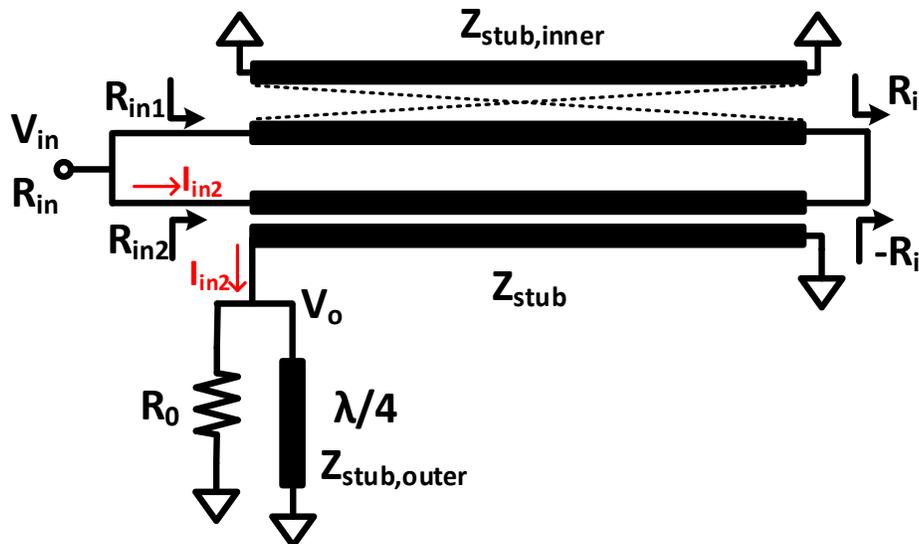


Fig. 5-10 Equivalent model of parasitic transmission line of the compensating stub

$$R_{in1} = \frac{\alpha^2}{\alpha+1} \cdot R_o, \quad (5-12a)$$

$$R_{in1} = \frac{\alpha^2}{\alpha+1} \cdot R_o, \quad (5-12b)$$

where α is defined as:

$$\alpha = \frac{Z_{stub,inner}}{Z_{stub}}. \quad (5-13)$$

Finally, the input impedance of the can be calculated:

$$R_{in} = R_{in1} \parallel R_{in2} = \left(\frac{\alpha}{\alpha+1}\right)^2 \cdot R_o \quad (5-14)$$

Equation (5-14) indicates input impedance is only a function of the ratio between $Z_{stub,inner}$ and Z_{stub} not their actual value. Comparing (5-14) and (5-8), as long as the ratio for $Z_{stub,inner}$ and Z_{stub} in the stub is retained at same the ratio for $Z_{o,inner}$ and Z_o in the coupled line ($\alpha = k$), the stub provides the reduced termination required by the coupled line (Fig. 5-8) to ensure an equal power split. This analysis is only valid for the electrical length of $\lambda/4$. Next, the performance over frequency sweep and an optimize k ($\alpha = k$), Z_{stub} and $Z_{o,outer}$, $Z_{stub,outer}$ to achieve minimum imbalance and widest bandwidth will be analyzed

Optimization is based on ADS simulation of the full Marchand Balun structure in Fig. 5-11 (refer to the appendix for calculations). Z_{stub} is first optimized with $k = 2$, $Z_{o,outer}$, $Z_{stub,outer}$ are kept sufficiently large (10 times Z_o). The Marchand balun in this design not only must provide balance-to-unbalance conversion, but also needs to provide a 1:4 impedance transformation (50 Ω single-ended output impedance to 200 Ω differential input impedance), which means the input

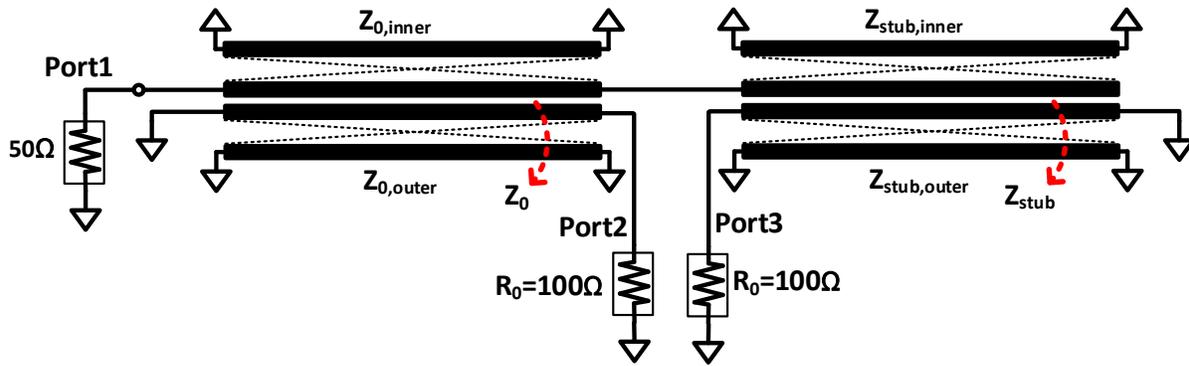


Fig. 5-11 Marchand balun schematic for ADS simulation

impedance in Fig. 5-8 must be a quarter of $2R_o$ ($R_o = 100 \Omega$). According to Eq. (5-9), the characteristic impedance of the couple line, Z_o , should be 100Ω . S-parameter simulation was performed at a center frequency of 1.15 GHz ($\lambda/4$ electrical wavelength) over a frequency span of 2GHz. The simulation results are plotted in Figs. 5-12 to 5-14. Figures 5-13 and 5-14 show the magnitude response and phase response over a range of Z_{stub} , where the minimum imbalance both in magnitude and phase are achieved when $Z_{stub} = Z_o$. Figure 5-13 is the result of the magnitude response at $Z_{stub} = Z_o$, which shows 134% fractional bandwidth can be obtained when measured at 1 dBc instead of 3 dBc as usual.

The second optimization was performed on k . In this optimization, Z_{stub} is set to equal Z_o (100Ω) with $Z_{o,outer}$, $Z_{stub,outer}$ kept large (10 times Z_o). The simulation results are shown in Figs. 5-15 and 5-16, which show a perfect balance can be maintained over the swept frequency as long as the ratio of $Z_{o,inner}$ to Z_o remains the same as the ratio of $Z_{stub,inner}$ to Z_{stub} , and Z_{stub} is equal to Z_o . A higher k is required to obtain wider bandwidth; however, a k higher than 2 does not provide a noticeable gain in bandwidth. Generally, a characteristic impedance above 200Ω is difficult to obtain for a transmission line (corresponding to $k=2$), a practical k would be below 2.

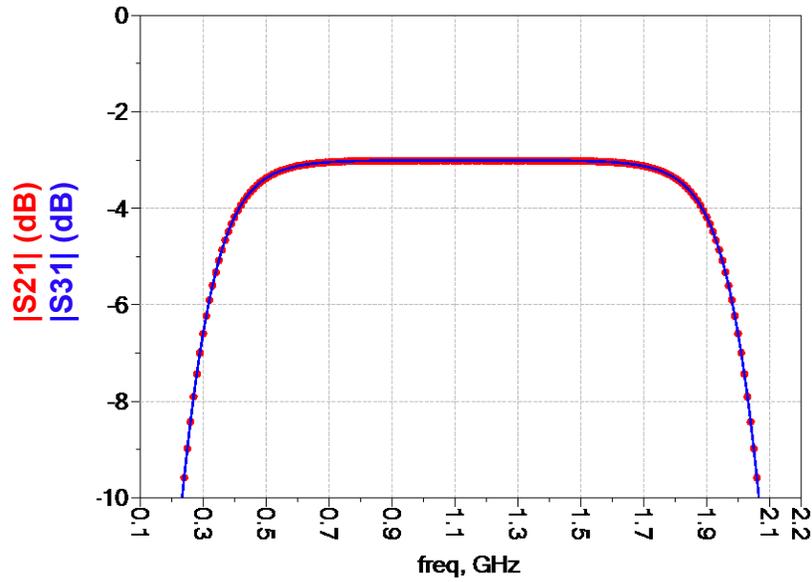


Fig. 5-12 Magnitude balance when $Z_{o,inner}/Z_o = 2$, $Z_{stub} = Z_o$, $Z_{o(stub),outer}/Z_o = 20$

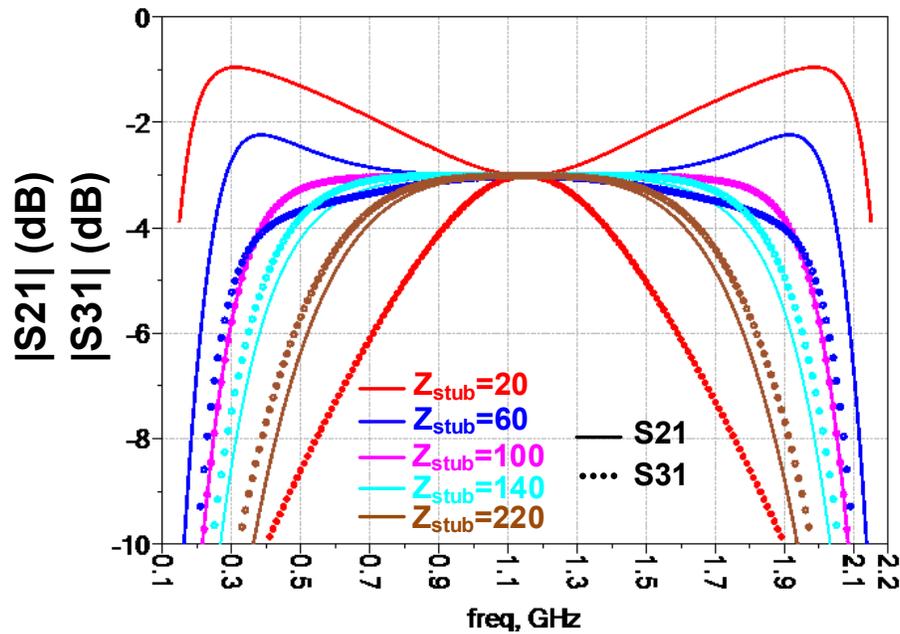


Fig. 5-13 Magnitude balance when $Z_{o,inner}/Z_o = 2$, Z_{stub} is swept, $Z_{o(stub),outer}/Z_o = 20$
 Fortunately, k of 1.5 is already sufficient to provide a fractional bandwidth of 128.7% (only 5% lower than the case when $k=2$).

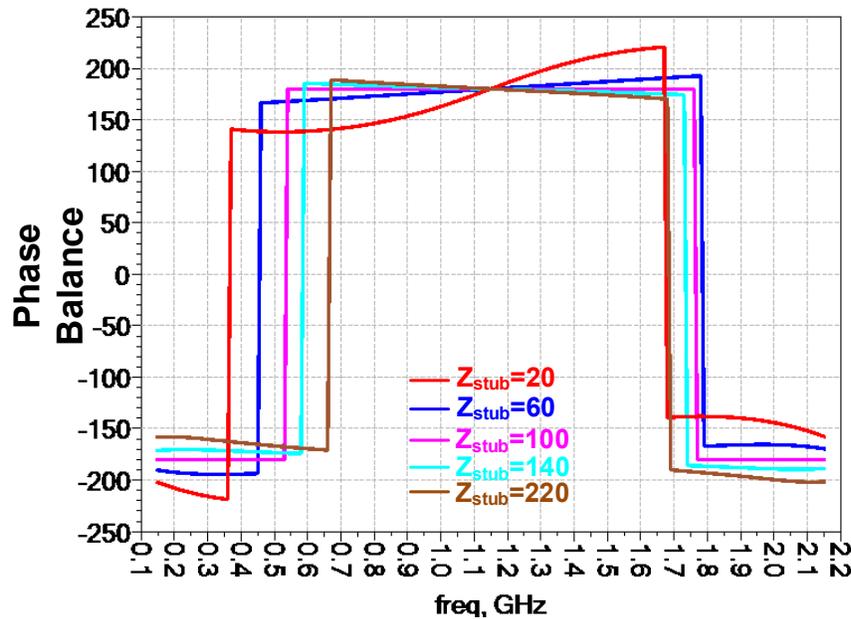


Fig. 5-14 Phase balance when $Z_{o,inner}/Z_o = 2$, Z_{stub} is swept, $Z_{o(stub),outer}/Z_o = 20$

The final parameters for optimization are the ratios for $Z_{o,outer}/Z_o$ and $Z_{stub,inner}/Z_{stub}$. To maintain a perfect balance over the swept frequency range, the above ratios should also be the same and are denoted by p . Simulation results are shown in Figs. 5-17 and 5-18, where the perfect balance is maintained when the ratios of $Z_{o,outer}/Z_o$ and $Z_{stub,inner}/Z_{stub}$ are the same. The effect of p on the bandwidth is quite similar to k . For practical design, a p of 1.5 may also be chosen to provide a fractional bandwidth of 120% (based on $k=2$).

According to this analysis, the Marchand balun should have a characteristic impedance of 100 Ω for both the main section (Z_o) and the stub (Z_{stub}) to transform 50 Ω standard load impedance to 200 Ω differential impedance seen by the transistors. The characteristic impedance of the parasitic transmission line ($Z_{o,inner}$, $Z_{o,outer}$, $Z_{stub,inner}$, and $Z_{stub,outer}$) should be as high as possible for the widest bandwidth. To obtain high characteristic impedance for the parasitic transmission lines, the width of the coupled lines in both the main section and the stub should be

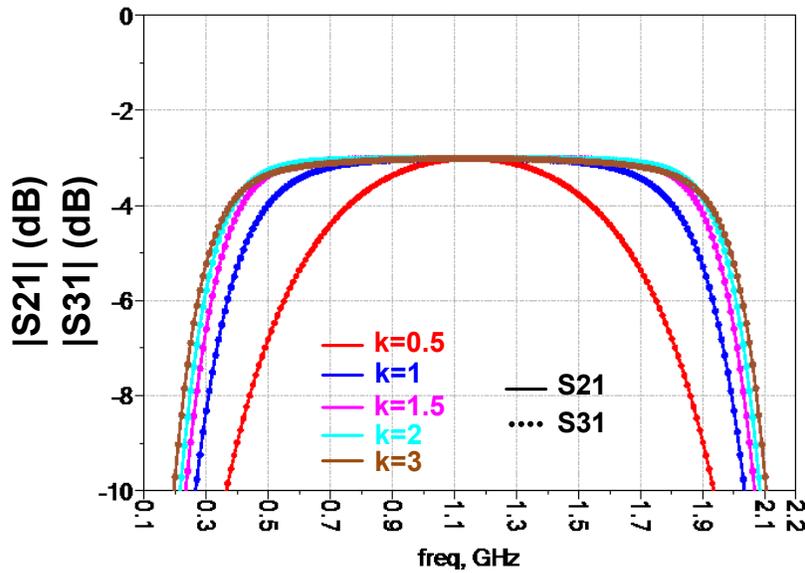


Fig. 5-15 Magnitude balance when $Z_{o,inner}/Z_o$ is swept, $Z_{stub} = Z_o$, $Z_{o(stub),outer}/Z_o = 20$

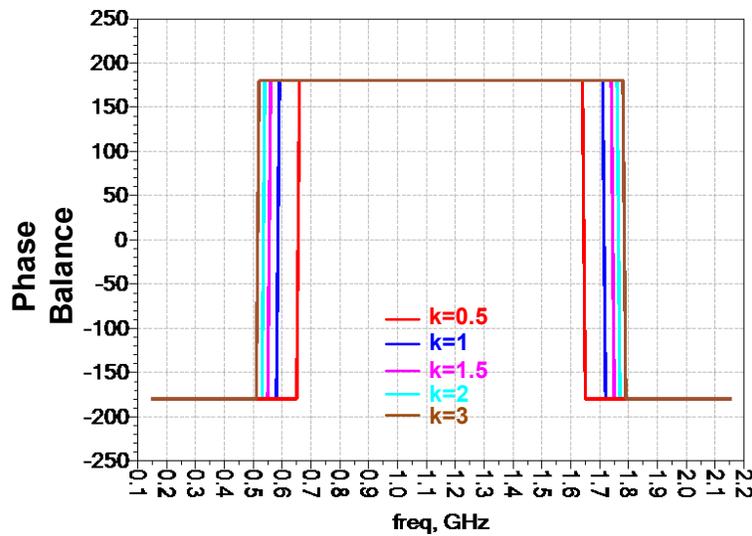


Fig. 5-16 Phase balance when $Z_{o,inner}/Z_o$ is swept, $Z_{stub} = Z_o$, $Z_{o(stub),outer}/Z_o = 20$

small (for a given ϵ and thickness of substrate). However, a smaller width will reduce the coupling factor of the coupled lines (increased Z_o and Z_{stub}). The coupling factor can be increased by reducing the space (increase C_m in Fig. 5-6(a)) between the coupled lines. However, the minimum space is limited to 10 mil which is not sufficient to obtain $100 \Omega Z_o$ or Z_{stub} with $Z_{o,inner}$, $Z_{o,outer}$ or $Z_{stub,inner}$, and $Z_{stub,outer}$ at least 1.5 times higher than Z_o . To break the tradeoff, we used a

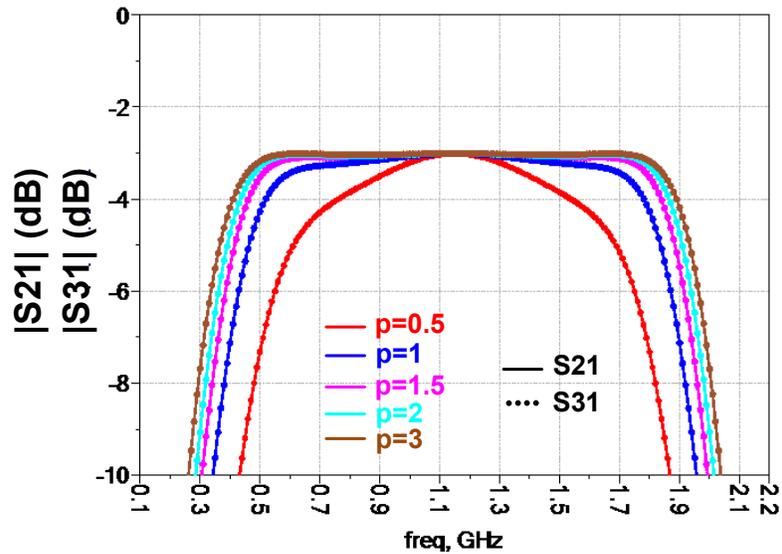


Fig. 5-17 Magnitude balance when $Z_{o,inner}/Z_o = 2$, $Z_{stub} = Z_o$, $Z_{o(stub),outer}/Z_o$ is swept

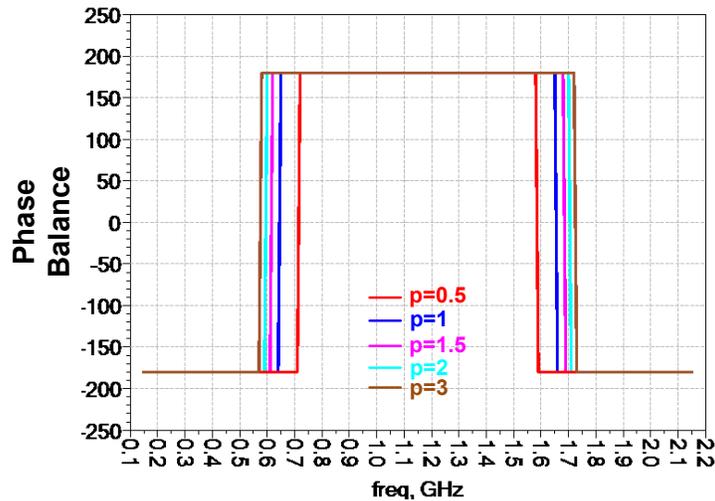


Fig. 5-18 Phase balance when $Z_{o,inner}/Z_o = 2$, $Z_{stub} = Z_o$, $Z_{o(stub),outer}/Z_o$ is swept structure depicted in Fig. 5-19 to increase the coupling and maintain $Z_{o,inner}$ and $Z_{stub,inner}$. To further increase the characteristic impedance of the parasitic transmission lines, the ground plane beneath the Marchand balun was etched away as shown in Fig. 5-19. The dimension for the final Marchand balun design is summarized in Table 5-1. The shorter length of outer line (L_{outer}) compared to the inner line is to compensate for vias connected to the ground plane. The length of the main section is also shorter than the stub. This compensates for the interconnection between

the main section and the stub, as well as some non-ideal effects as frequency goes higher. This layout was simulated using a Momentum simulator in ADS.

The layout was simulated using Momentum simulator in ADS. Simulation results are plotted in Fig. 5-20(a) and summarized in Table 5-2. The values in Table 5-2 are obtained within the fractional bandwidth. Fig. 5-20(b) presents the comparison between EM simulation and ideal simulation using the schematic in Fig. 5-11 with $Z_o = 100 \Omega$, $Z_{o,inner}/Z_o = 1.5$, $Z_{stub} = Z_o$, and $Z_{o(stub),outer}/Z_o = 1.5$. It can be seen that the EM simulation results agree well with the previous analysis.

Table 5-2 Marchand Balun Dimension

	L_{inner} (mil)	W_{inner} (mil)	L_{outer} (mil)	W_{outer} (mil)	S(mil)
Main Section	1711.1	54	1690	10.5	11
Stub	1774.6	54	1730	10.5	11

Table 5-1 EM Simulated Result of Marchand Balun

	Min.	Max	870MHz	1.48GHz
Mag. Imbalance (dB)	0	0.22	0.093	0.004
Phase Imbalance (degree)	0.002	0.9	0.082	0.67
Loss (dB)	-0.153	-0.442	-0.154	-0.167
Fractional Bandwidth	117% centered at 1.175GHz			

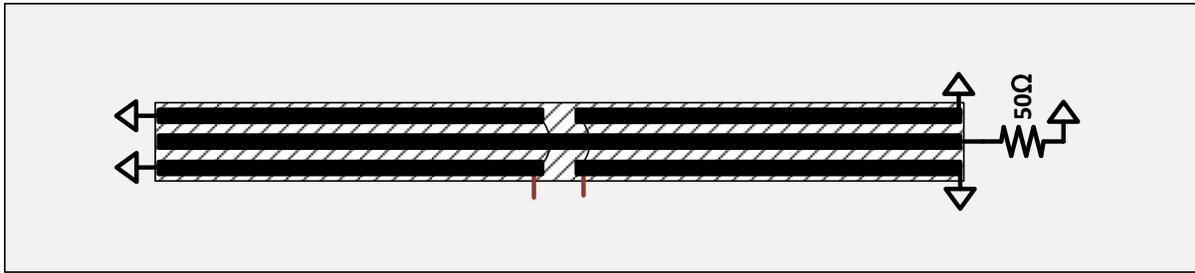
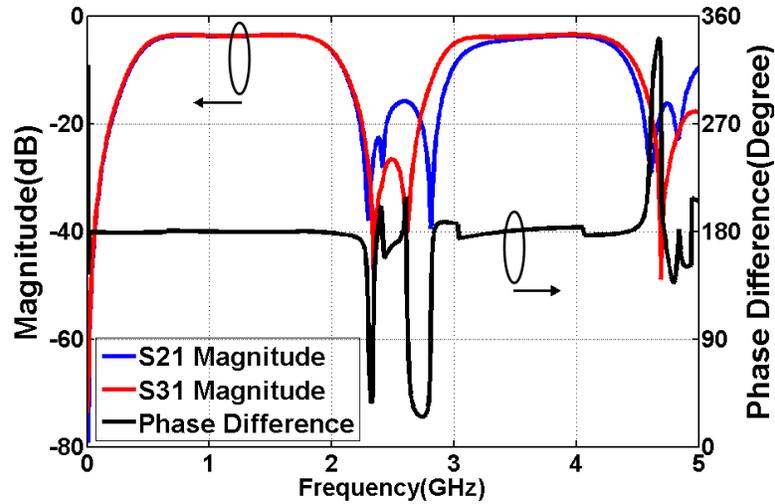
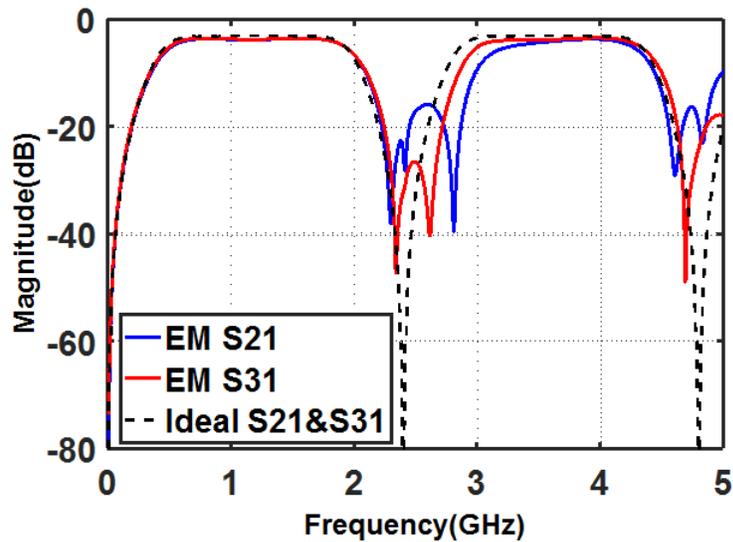


Fig. 5-19 Ground-defected Marchand balun



(a)



(b)

Fig. 5-20 Balun simulation results (a) EM simulation only (b) comparison between EM simulation and ideal simulation

5.4. Load Network Design

Based on the differential and common-mode impedances of the broadband Marchand balun, the remaining part of the load network (Fig. 5-5) was designed to realize the impedance described in Fig. 5-4. The rest of the load network, A and B, comprise a differential section (A_{DM}, B_{DM}), for terminating the fundamentals and IM3 components, and a common-mode section (A_{CM}, B_{CM}), for terminating the 2nd-harmonics and IM2 components. Because the common-mode portions of the matching networks are connected to AC ground, they do not impact the impedance of the differential signals.

The balun feedline is necessary for each differential port of the balun to reach section A. It has the same electrical length as the Marchand balun which is a quarter wavelength at 1.175 GHz. The characteristic impedance of the feedline was chosen in a way the differential impedance at f_1 (870 MHz) and f_2 (1.49 GHz) were flipped on the Smith chart with respect to the real-impedance axis. Such feedlines do not impact the real components of the fundamental impedance, but their imaginary parts change their sign from positive to negative.

The differential part of section A, A_{DM} , provides two resonant frequencies that detune at f_L and f_H and cancels the imaginary part of the fundamental impedance present at the balun feedline node resulting in real impedance of 200 Ω differentially. The dual-band resonance also provides a low impedance for 3rd-order IM components to eliminate any real parts that may come from the balun. Any real impedance at harmonics or IM components will increase loss in the load network. The inter-connect trace has a characteristic impedance of 100 Ω ; thus, they will not affect the fundamental impedance. This capacitor provides a DC blocking as well as capacitive impedance at $2f_L - f_H$ (260 MHz); thus, bringing it below the short node on the Smith chart as

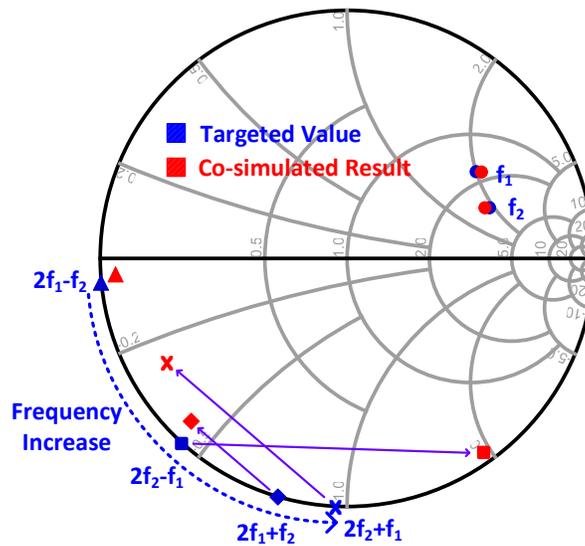
shown in Fig. 5-4. The inter-connect trace also provides some electrical length to $2f_H - f_L$, $2f_L + f_H$ and $2f_H + f_L$ and brings them to the capacitive half plane on the Smith chart, making the design of section B easier.

The differential component of section B provides the required inductive susceptance to the real fundamental admittance presented by the foregoing part of the load network and bring the fundamental impedance to the target values as shown in Fig. 5-4. It also adjusts impedance at all four 3rd-order IM components and moves them as close to the target values as possible.

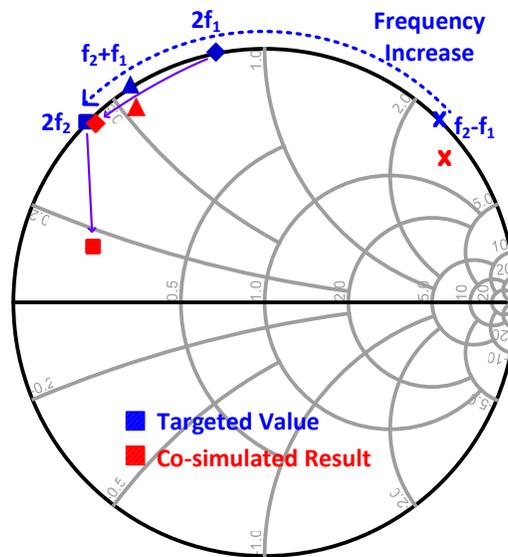
Target impedance of 2nd-order harmonics and IM components are realized by common-mode matching sections, A_{CM} and B_{CM} . Since they are attached to the virtual ground nodes of differential parts, they won't affect differential impedance of the load network. After optimizing the design of A_{CM} and B_{CM} , the overall load network was designed using Rogers RO3203 with 30 mil thickness and 1 oz. copper cladding as the substrate. Keysight's ADS Momentum was then used to simulate the complete load network and the results are plotted in Fig. 5-21. The shifts in the simulated impedance for the IM3 components seen in Fig. 5-21(a) is not too significant as this will cause on a small drop in the drain efficiency. The shift in the real-part of the 2nd-harmonic impedance seen in Fig. 5-21(b) is more problematic than the reactive shift, and this will be discussed more in Section 5-7.

5.5. Input Network Design

The input network contains input balun, a stabilizing network, and an input matching network. The stabilizing network was directly connected to the gate of transistors and unconditionally stabilized the transistors, which guaranteed an unconditional stable for the whole



(a)



(b)

Fig. 5-21 EM cosimulated load impedance profile (a) fundamentals and 3rd IMs (b) 2nd harmonics and IMs

PA regardless what was added afterwards. Figure 5-22 shows the schematic for stabilizing the network. The series connection for parallel RC and parallel RL provide sufficient series loss at low and high frequencies without sacrificing too much power gain degradation in the band. The shunt

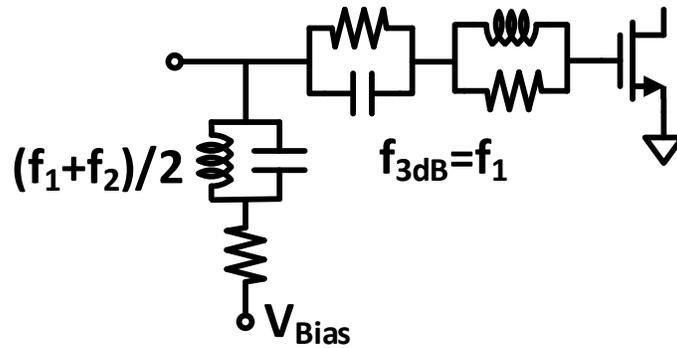


Fig. 5-22 EM cosimulated load impedance profile (a) fundamentals and 3rd IMs (b) 2nd harmonics and IMs

loss network contains an LC resonator resonating around the middle of f_L and f_H , providing a similar function as the series loss network.

Two transistors with the stabilizing networks are combined differentially with a Marchand balun. The design of the input balun does not need to provide impedance transformation. Thus, it is easier than the design of the output balun. Source pull simulation was then performed with the input stabilizing network and the input balun to determine optimal input impedance at f_L and f_H . An input matching network was designed to match 50 Ω source impedance to the optimal input impedance.

5.6. Measurement Results

The PA was fabricated on Rogers RO3203 with 30 mil thickness and 1oz copper cladding. The power transistors are implemented using CGH40006P GaN HEMT from Cree and all passive LC elements are implemented using SMT components from Murata. The complete PA occupies a board area of $10.2 \times 12.7 \text{ cm}^2$ and is pictured in Fig. 5-22. The DC supply voltage was set to 18 V and the gate bias voltage was set to -1.9 V with respect to the source for approximately 1.5 V overdrive with respect to a threshold voltage of -3.4 V. This guarantees that the transistors are

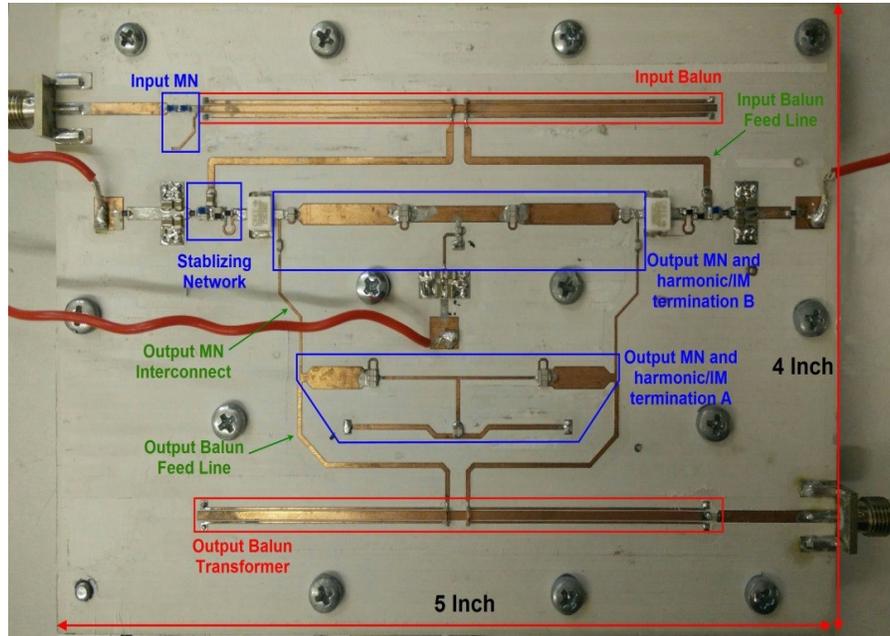


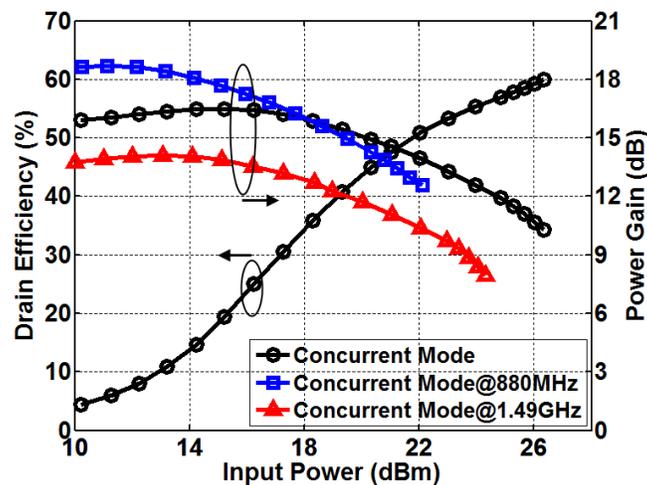
Fig. 5-23 Prototype of proposed concurrent dual-band class D PA

biased in the triode region. The 870 MHz and 1.48 GHz concurrent dual-band input signal was generated by combining the output of two RF signal generators through a wideband diplexer. The test setup was controlled by computer through GPIB ports and automatic measurement was realized with matlab script.

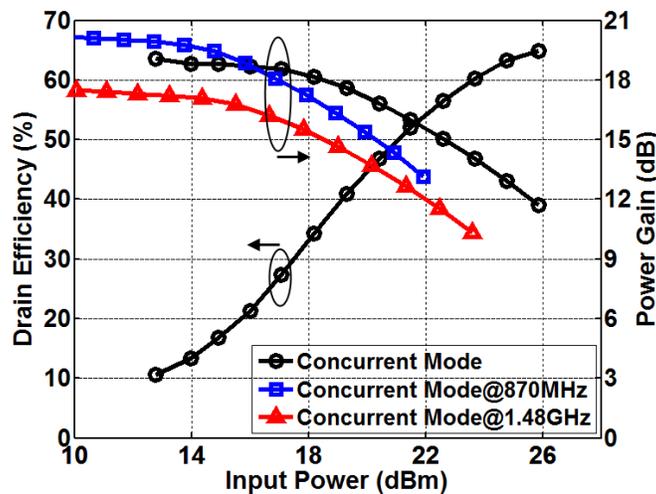
First measurement was done with input power sweep at both concurrent mode and single mode. Fig. 5-24~ Fig. 5-25 shows the measured and simulated efficiency, output power and gain in concurrent mode. A measured drain efficiency of 60% was achieved in concurrent mode at about 6dB overdrive as shown in Fig. 5-24(a) which is only about 5% lower than simulated result under same overdriven level (Fig. 5-24 (b)). However, measured power gain is 1.5 dB lower in low band, 3.5 dB lower in high band and 2.5 dB lower in concurrent mode compared to simulated results. This is due to lower fundamental impedance of the load network after fabrication. Because of the increased gain difference in the two bands, output power difference between the two bands

in concurrent mode increases from 1 dB to 2.4 dB. Total measured output power at 6 dB over drive is around 36.7 dBm which is 0.9 dB lower than simulated output power, 37.6 dBm (Fig. 5-25).

The single-mode drain efficiency can be observed in Fig. 5-26, which plots drain efficiency as a function of the input power ratio of the low band over high band, $P_{in,low}/P_{in,high}$. The PA stayed at 6 dB over drive over the power balance sweep. The black curve on Fig. 5-26 shows the simulation results with a numerical load tuner that provides the load impedance as required in Fig.



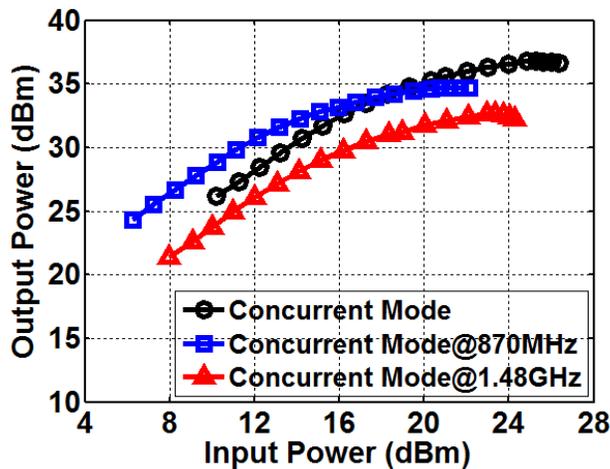
(a)



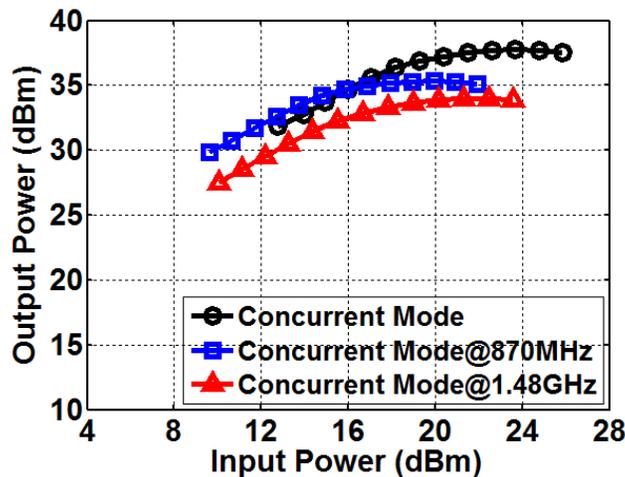
(b)

Fig. 5-24 Drain efficiency and power gain (a) measured (b) simulated

5-4. The blue curve is the simulation result of the EM model for on-board traces, including baluns and actual lumped LC component models. Both simulations used actual transistor models from Cree. The red curve is the measured result. The first simulated result (black) shows the expected results for our proposed concurrent dual-band switch-mode PA where both single-mode and balanced concurrent-mode drain efficiency stay high at 83.5% and 76.4%, respectively, (considering power loss in the actual transistors) and with only about a 7% efficiency drop from the single mode to the concurrent mode. Both EM co-simulation results show an unexpected



(a)



(b)

Fig. 5-25 Output power (a) measured (b) simulated

imbalance between the low and high bands. The lower drain efficiency at the high band is due to the impedance shift in both the real and the imaginary parts at the 2nd harmonic of high band, $2f_H$ as shown in Fig. 5-21(b). Compared to the impedance shift at $2f_L$ in Fig. 5-21 (b), there is more shift in the imaginary part and a significant increase in the real part of the impedance at $2f_H$. The shift in the imaginary part introduces a power loss in the transistors, while an increase in the real part will cause a power loss on the 2nd harmonic, $2f_L$. Measured results show a greater drain efficiency imbalance between the low and high bands, which is possibly due to more shift in the 2nd-harmonic impedance of the high band after the PA was fabricated. A fundamental impedance shift at f_H will also play a role in the efficiency degradation at the high band. The drain efficiency increase at the low band indicates the fundamental and 2nd-harmonic impedance at low bands were shifted toward the required value on Fig. 5-4 after fabrication. The measured drain efficiency was only about 5% lower than for the EM co-simulation results in the concurrent mode.

Figure 5-27 shows the simulated and measured drain efficiencies as a function of gate bias voltage. Like Fig. 5-26, the black curve shows the simulation results with a numerical load tuner that provides exact load impedance as required in Fig. 5-4. The EM co-simulation results are plotted with a blue curve and the measured results are the red curve. All results are under the 6dB over drive. The first simulation results (black) show a significant drain efficiency drop, since the transistors are biased at the lower gate voltage (bias into saturation region), demonstrating the gate bias effect in section 4. However, bias at the higher gate voltage (further into the triode region) does not bring a higher drain efficiency. An optimal bias point exists in the triode region. A detailed analysis of the bias in the deep triode region is not the scope of this paper. EM co-simulation and

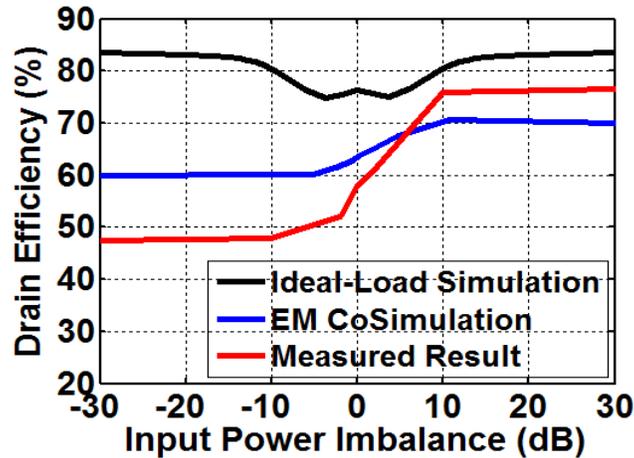


Fig. 5-26 Drain efficiency versus gate over drive voltage

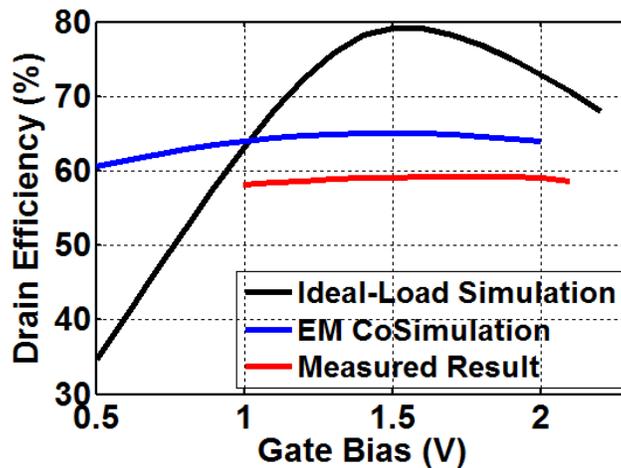


Fig. 5-27 Drain efficiency versus input power balance

measured results do not show noticeable gate-bias effects, due to their load impedance shift at the even-order harmonics and IM components (Fig. 5-21(b)).

Shifts cause the impedance seen by the transistor intrinsic drain node to move from an ideal value (open for even-order harmonics and IM components), thus, reducing the peaks in the drain-source voltage as shown in Fig. 4-9. The further away from the ideal value, the less gate-bias effect the PA will have. Such explanation can be verified with Fig. 4-8, where a smaller number of proper harmonic termination causes less gate bias effect. However, the drain efficiency at the optimal bias

Table 5-3 State-of-the-Art Concurrent Dual-band Power Amplifiers

	f (GHz)	Pout (dBm) @ Single Mode	Pout (dBm) @ Concurrent Mode*	Efficiency @ Single Mode	Efficiency @ Concurrent Mode**	Signal
[64]	1.96/3.5	39/40	36.5	57%/49.5% ‡	44.1% ‡	CW
[65]	1.8/2.4	35.5/35.5	33	34.7%/32.7% ‡	24.7% ‡	WCDMA/LTE
[66]	1.8/2.4	36.2/34.5	33.4	54.2%/40.7% ‡	34.4% ‡	LTE/WiMAX
[68]	0.85/2.33	44/42.5	31.4	60%/53% †	26.7% †	CW/LTE***
[69]	1.9/2.6	41.5/41.2	39.5	73%/67.5% †	56% †	CW
This Work	0.88/1.49	37/36	36.7	48%/76.5% †	60% †	CW

* Total output power, ** Total efficiency, *** CW for single mode, LTE for concurrent mode, † Drain efficiency, ‡ PAE

point will decrease as impedance shifts away from their required values. Finally, a comparison between this work and other state-of-the-art concurrent dual-band PAs is summarized in Table 5-3. The proposed concurrent dual-band class-DF-1 PA shows promising efficiency and output power performance in the concurrent dual-band operations than other PA topologies. However, lower drain efficiency was observed in the high band, due to its 2nd-harmonic impedance shift both in the real and imaginary parts that increase power loss in the 2nd-order harmonic and transistors, respectively.

5.7. Conclusion

This chapter presents the actual implementation of the proposed PAs. Especially a broadband Marchand balun with 1:4 impedance transformation ratio was designed. Equations guiding the behavior of the Marchand balun was derived with further bandwidth optimization using ADS simulation. Based on the balun, a differential load network was then created to properly terminate two fundamental frequencies, four 2nd IM components/harmonics and four 3rd IM components. The PA was fabricated and measured in lab and showed record efficiency among existing concurrent dual-band PAs.

CHAPTER 6. FUTURE WORK: LINEARITY ENHANCEMENT FOR CONCURRENT DUAL-BAND SWITCH-MODE POWER AMPLIFIERS

6.1. Introduction

The proposed concurrent dual-band current-switching class-D PA presented in Chapters 4 and 5 can provide higher efficiency and output power compared to concurrent dual-band PAs in linear topologies (class A, class B, etc.). However, the gains of higher efficiency and output power come from over-driving the PA, which will introduce linearity problems. In single-band PAs, when PAs are over-driven (switch-mode PA) for higher efficiency, LINC techniques usually come along to maintain linearity performance. LINC (Linear Amplification using Nonlinear Components) describes linear PA systems using nonlinear PAs. These techniques include out-phasing (Chireix), envelope elimination restoration (EER) or polar PA, class S PA ($\Delta - \Sigma$ modulation PA), and so on [24].

In this chapter, some linearity problem in a concurrent dual-band switch-mode PA will be discussed and differences from single-band PAs will be noted. Some possible techniques will then be proposed that are suitable using the LINC technique for concurrent dual-band switch-mode PAs. Detailed evaluation and development of LINC techniques need more effort and will be a future work of the concurrent dual-band class-D PA developed in this thesis.

6.2. Linearity Issues in Concurrent Dual-Band Switch-Mode Power Amplifiers

When an envelope-modulated signal goes through a non-linear single-band power amplifier (over driven), spectrum regrowth is observed as shown in Fig. 2-7 and base-band signal is distorted. However, for constant-envelope and phase-modulated signal, there is no spectrum regrowth, meaning base-band signal (modulated into phase) is not distorted. The fact phase modulation remains contaminated in a nonlinear PA is the base for using the LINC technique where switch-mode PAs are used, while linear amplification is realized.

In a concurrent dual-band nonlinear power amplifier, it becomes more complicated because of the large number of inter-modulation components generated. Figure 6-1 shows part of the spectrum that could cause interference when the frequency ratio between high and low bands is

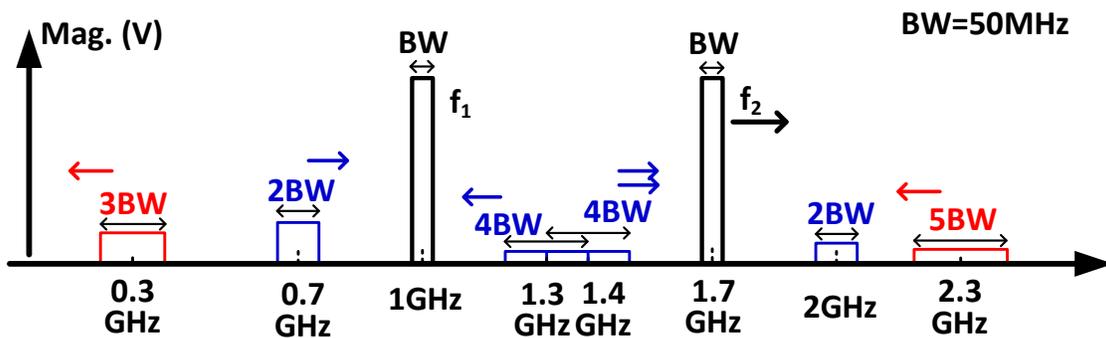


Fig. 6-1 Spectrum in a concurrent dual-band nonlinear power amplifier with frequency ratio of 1.7

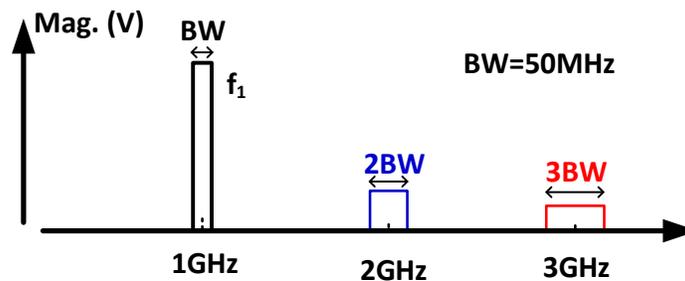


Fig. 6-2 Spectrum in a dual-band nonlinear power amplifier with constant-envelope phase-modulated signal

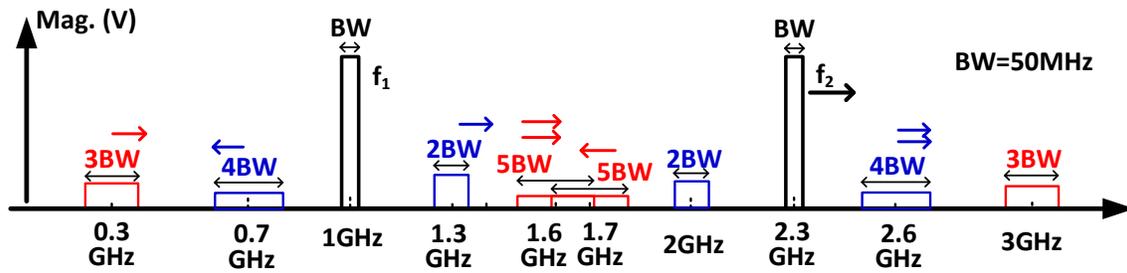


Fig. 6-3 Spectrum in a concurrent dual-band nonlinear power amplifier with frequency ratio of 2.3

equal to 1.7. As discussed in Chapter 3 and 4, Fig. 6-1 shows more IM components than harmonics in the spectrum and these IM components may cause base-band signal distortion in the LINC system. It was presented in Section 2.4.3 that an envelope-constant phase-modulated signal can be amplified linearly using nonlinear Pas, due to the feature that phase information will be reserved through a nonlinear PA. In terms of the spectrum, this feature means no spectrum regrowth around the fundamental carrier as indicated by Fig. 6-2 (compared with Fig. 2-7). However, harmonics with wider bandwidth are generated still. The zero-regrowth of the spectrum also applies to concurrent dual-band PAs as shown in Fig. 6-1 where no spectrum regrowth is observed around the two carriers (f_L and f_H). However, unlike the single-band case, in concurrent dual-band nonlinear PAs, many IM components are generated and may fall onto or become too close to the fundamental bandwidth to be filtered if the frequency ratio is not chosen properly. Therefore, this will cause distortion to the base-band signals. Figure 6-1 shows the problematic IM components and harmonics (to the 5th-order nonlinearity) for the frequency ratio of 1.7. Note, all IM components and harmonics are sufficient distance from the fundamental signal bands and will not distort the base-band. Hence, they should be filtered without too many difficulties. The frequency ratio of 1.7 is probably the best choice below 2, since as the ratio increases or decreases (f_H

increases or decreases), IM components or harmonics move closer to the fundamental signal bands and become more difficult to filter.

Frequency ratios above 2 provide more choices as shown in Fig. 6-3. From a ratio of 2.3 to 2.7, there is more distance between IM components/harmonic and fundamental signal bands than the best case shown in Fig. 6-1. As frequency ratio increases (above 3, 4, etc.), more choices of frequency ratios are expected that have sufficient distance between IM components/harmonic and fundamental signal bands.

6.3. Review of Linearity Enhancement Techniques

After discussing linearity issues in the concurrent dual-band switch-mode PAs, it is worthwhile to review the existing techniques or topologies often utilized to improve power amplifier linearity. In the remainder of this chapter, different linearity/efficiency enhancement techniques will be presented first and then evaluated to determine the best, suitable technique for concurrent dual-band switch-mode PAs.

6.3.1. Class-H, -G, and Envelope Tracking

Class-H, class-G, and the envelope-tracking (ET) technique are included in the same category, since they improve efficiency through a modulated power supply [88]. Class-H is the ideal in audio power amplifiers where the power supply is modulated with a signal envelope. This becomes the ET technique in RFPAs, which is more challenging, due to a higher bandwidth of modern data (40MHz in LTE-A). Class-G PA is halfway from the constant power supply to full envelope tracking, since it provides multiple fixed power supply levels according to the input power envelope; thus, greatly reducing the requirement for power modulators. The simple power supply level switching allows class-G PA to employ DC-DC converters to provide a higher

efficiency than linear converters used in envelope tracking. However, the class-G PA loses power as PAR and the data bandwidth increases.

6.3.2. Doherty Power Amplifiers

Another method to improve the average efficiency of the linear power amplifier is to modulate load impedance instead of modulating the power supply [24, 89, 90]. By adding another PA (auxiliary PA) to drive the same load impedance in phase and a $\lambda/4$ -TLine impedance converter, the effective load impedance seen by the main transistor is reduced, since it becomes over driven (which is also the time the auxiliary PA is turned on). The result is the main PA is kept at full swing (not further compressed) as the input power further increases. Based on the number of auxiliary PAs, the high-efficiency range (main PA keeps at full swing) can be 6 dB (one auxiliary PA) or 9 dB (two auxiliary PAs), which usually covers the PAR of a LTE signal (6~10 dB).

The advantage of Doherty PA compared to power supply modulation is the Doherty PA does not require an extra power converter, which is low efficiency if a large bandwidth is needed. The main concern for Doherty PAs is the limited RF bandwidth [91]. In addition, the design becomes too complex as more auxiliary PAs are added to cover the higher PAR.

6.3.3. Class-S Power Amplifiers

In a class-S PA, the modulated signal (envelope varying) is converted to pulse-width modulated signals using a band-pass Δ - Σ modulator [92, 93]. Since the pulse-width modulated signal is simply a two-state signal, a class-D PA is usually utilized to amplify it. At the output of the PA, the original envelope-varying signal will be restored through a band-pass filter. Theoretically, class-S PA is not restricted to the type of modulations or how many carriers in the

signal; thus, it is suitable for concurrent multi-band operation. However, class-S PA is restricted to lower frequencies below GHz, since an oversampling frequency is required for the Δ - Σ modulator. The record frequency (carrier) for class-S PAs is about 500 MHz, published around year 2010 [93].

6.3.4. Polar/Envelope Elimination Restoration (EER) Power Amplifier

Envelope elimination restoration was first proposed by Kahn [94]. Thus, it is also called Kahn EER. This technique looks similar to ET PAs in the sense the power supply is modulated with a signal envelope in both cases. They are essentially different. For ET PA, the power amplifier works in a linear region (barely compressed) and the signal processed in the PA is completed in terms of magnitude and phase information. The quality of a modulated power supply will affect the average efficiency, but barely distorts the signal. On the other hand, EER PAs work in hard compression (switch mode) and the signal processed in the PA only contains phase information. Magnitude information is added to the signal through power supply modulation [24, 94-96]. Thus, in EER PA, the quality of the modulated power supply (mostly a delayed mismatch between PA path and power converter path) will directly translate into signal distortion. Modern approaches to EER do not have an envelope detector and limiter any more. The envelope signal and phase modulated signal are generated in the digital processor, and given a new name— polar PA.

Polar PAs feature high efficiency and an ability to operate at much higher frequencies than the class-S PA. The generation of magnitude envelope and phase-modulated signal in the digital processor is also not computation power consuming (compare to out-phasing PA). The limitation of polar PA comes from the bandwidth and efficiency limitation of its power converters [97, 98]. A more precise envelope signal is required than for the case of ET PA..

6.3.5. Outphasing Power Amplifier

Outphasing was dated back in the 1930s. First proposed by Chireix [99], it is also called the Chireix technique. The out-phasing technique uses simple trigonometric equations to modulate magnitude information into a phase [99-101]:

$$\begin{aligned}
 S_{in}(t) &= A(t) * \cos(\omega t) \\
 &= \cos\left(\cos^{-1}(A(t))\right) * \cos(\omega t) \\
 &= \cos\left(\omega t + \cos^{-1}(A(t))\right) + \cos\left(\omega t - \cos^{-1}(A(t))\right) \quad (6-1)
 \end{aligned}$$

Equation (6-1) shows the amplitude signal becomes a pair of opposite phase signals in two constant envelope sinusoidal signals.

The out-phasing technique does not need power converters like the polar PAs. Therefore, this technique is not limited to the constrained bandwidth and efficiency of power converters. It can also operate at higher frequencies as opposed to class-S PA. However, the signal bandwidth was largely increased after the out-phasing technique and requires a switch-mode PA to provide a wider bandwidth. Also, the out-phasing technique needs high-speed digital computation, which is expected a lesser problem as computation power continues to increase

6.4. Maintain Linearity with Out-Phasing Technique

Techniques presented in Section 6.3.1 and 6.3.2 are used to improve efficiency under linear region, thus not suitable for linearity improvement for switch-mode PAs. Section 6.3.3 and 6.3.4 presented three LINC techniques available to maintain linearity, while using a switch-mode PA. The first technique, class-S power amplifier, uses a band-pass Δ - Σ modulator to convert the

envelope-varying signal into a two-state signal that can be amplified by a switch-signal with high efficiency. The original signal is then restored through a band-pass filter. The problem with this method resides in the over-sampling requirement, which makes it only useful in a lower frequency range (<1GHz). However, the proposed concurrent dual-band PAs are targeted at a higher GHz range. In the lower than GHz range, current frequency bands can be covered by a wideband PA and no concurrent dual-band PAs are required. In addition, the pulse-width modulated signal after the Δ - Σ modulator has more frequency components than simple 50% duty cycle square signals. Therefore, it requires proper load impedance terminations on more frequency components and dramatically increases the design difficulty of the switch-mode PA. Reference [93] showed efficiency dropped from 70 to 40% when the signal changed from 50% duty cycle square waveform to pulse-width modulated waveform.

The polar PA (EER technique) works at a much higher frequency range and does not have a problem of dealing with more frequency termination as in class-S PAs. However, the polar PA is unable to support concurrent dual-band operation in the sense the envelope information for each band can be distinguished at a high-level modulation:

$$A_1(t) \cos(\omega_1 t) + A_2(t) \cos(\omega_2 t) \neq (A_1(t) + A_2(t)) * (\cos(\omega_1 t) + \cos(\omega_2 t)) \quad (6-2)$$

The right-hand side of Eq. (6-1) shows the high-level modulation (power supply modulation) on the concurrent dual-band signal. It is clear $A_1(t)$ (envelope of first band) and $A_2(t)$ (envelope of first band) are unable to be distinguished and assigned to each carrier.

The final method, the out-phasing technique, is a promising choice to realize LINC with concurrent dual-band switch-mode PA. It can work at a higher frequency range as a polar PA and

can restore envelope information for each band, since the envelopes are stored in the phase of each carrier and delivered to output without distortion. Although the out-phasing technique requires more digital processing power, it should not be a big problem, since commutating power for the DSP continues to increase rapidly, due to further scaling of CMOS technology and more advanced architecture. However, one problem of the out-phasing technique should be studied to better evaluate its benefits in concurrent dual-band switch-mode PAs. With the envelope modulated into phase, the bandwidth for each carrier increases and the bandwidth of harmonics/IM components may reduce the frequency distance between fundamental signals and harmonic/IM components as discussed in section 6.2. However, this is not to be a problem, since it is known the fundamental signal bandwidth restores to its original width after out-phasing signals combine at output. Harmonic and IM components may also have the same behavior. Rigorous derivation is required before any claim can be made.

CHAPTER 7. CONCLUSION

As wireless standards continue to evolve from 3G and 4G to the forthcoming 5G, more frequency bands in higher frequency ranges (~6 GHz, 30 GHz, 60 GHz, etc.) must be covered by power amplifiers in the RF front-end module (RF FEM). Current solutions, which use one power amplifier to cover several adjacent frequency bands, will soon become impractical as frequency bands expand into higher frequency ranges, due to constricted areas and cost of RF FEM. In addition, carrier aggregation, a standard feature in 4G and 5G to increase data rate, requires extra filters (Fig. 1-4) in addition to duplexers for FDD, if old front-end structures are utilized. A multi-band PA capable of supporting multi-carrier (non-adjacent) operations simultaneously will reduce the number of PAs and filters used in the RF front-end and, therefore, reduce cost, area, and power loss introduced by extra filters, allowing future RF FEM to cover more frequency bands.

Unfortunately, traditional multi-band power amplifiers are designed for operating one carrier at one time and do not consider intermodulation components (IM components)—only harmonics. Although they can achieve good efficiency at each band separately, they fail to provide a good performance in the concurrent mode (multiple-carrier operation simultaneously) as in the single mode (one carrier at a time). In fact, the efficiency and output power degradation are significant [67-71]. The mechanism behind this degradation was largely unexplained until recently, when researchers presented a detailed efficiency analysis of concurrent dual-band linear PAs [72-74]. In [72, 73], a concurrent dual-band class-B PA was designed with shorting significant harmonics and IM components to ground. However, this method still suffers a 16% drain efficiency drop and 3 dB output drop. To be useful in future RF FEMs, both efficiency and output power must be improved.

In single-band PAs, switch-mode operation with proper harmonic termination can improve both efficiency and output power as discussed in section 2.4.2. In this thesis, such an idea was applied to concurrent dual-band PAs with the purpose of achieving comparable efficiency and output power in the concurrent mode as in single mode. However, the theory of concurrent dual-band switch-mode PA is not readily applicable from single-band switch-mode PAs. The theory and design methodology must be developed before a concurrent dual-band switch-mode PA can be designed.

In this research, a concurrent dual-band class-D PA was developed from fundamental theory, including its behavior and theoretical performance; design methodology, including bias requirement and finite termination discussion; to actual implementation and measurement results. The theoretical analysis shows the concurrent dual-band class-D achieves about 87% drain efficiency in the concurrent mode with infinite harmonic/IM termination at 6 dB over drive, which is only 5% lower than the single-mode case (92% drain efficiency). The efficiency improvement is significant compared to the concurrent dual-band class-B PA where the theoretical maximum concurrent-mode drain efficiency is about 62.5%, which is 16% lower than the single-mode case. The output power drop in the concurrent operation is also minimized to about a 1.2 dB at 6-dB over drive in the concurrent dual-band class-D PA compared to about a 3 dB drop in the concurrent dual-band class-B PA.

Bias is critical in the design of the class-D PA, for both concurrent dual-band and single-band cases. It was determined a high bias (bias in triode region, or bias above class A) is necessary to avoid efficiency degradation. If bias is low (bias in saturation), then spikes appear to drain the voltage waveform causing more power dissipation in the transistor and reduce efficiency. The bias

analysis in this thesis is from a perspective of time-domain waveform, a frequency domain analysis can be found in [40].

The harmonic/IM termination required by the proposed concurrent dual-band class-D PA is more complicated than the single-band class-F-1 PA, where usually only 2nd and 3rd-order harmonics are considered. However, in the proposed PA, there exist a total of 10 harmonics/IM components even though only to 3rd-order nonlinearity are considered. This dramatically increases the design complexity of the load network, which may increase area and loss of the load network. Fortunately, minimal efficiency can be sacrificed to greatly reduce design complexity. Section 4.5.2 determined the worst termination on 3rd harmonics causes a very small reduction (80 to 76%) in single mode and almost no reduction in the concurrent mode. Furthermore, removal of the proper termination on all four 3rd-order IM components only causes about a maximum 10% drop in drain efficiency. If design complexity or area is a big concern, 3rd IM components can also be (or partially) left unconsidered with several percentage drops in drain efficiency. Second harmonics and IM components should always be properly terminated to avoid significant efficiency drops either in the single mode (fail to terminate 2nd harmonic) or the concurrent mode (fail to terminate 2nd IM components).

A differential load network was proposed to realize the load termination requirement with reduced design complexity, since it can provide differential impedance and common-mode impedance independently. A broadband balun transformer (1:4) was theoretically developed and optimized for minimum imbalance and maximum bandwidth to combine the differential signal to the single-ended 50 Ω load. The proposed PA was fabricated and measured in laboratory, and achieved a concurrent-mode drain efficiency of 60%—among the best of existing concurrent dual-

band PAs. Single-mode efficiency was quite unsymmetrical with a much higher drain efficiency in low band (76.5%) than high band (48%). The low efficiency for the high band came from its 2nd-harmonic impedance shift both in real part and imaginary part that increase power loss in the 2nd-order harmonic and transistors, respectively. Nevertheless, measurement and simulation results together demonstrated the proposed concurrent dual-band class-D have the capability to achieve a much higher concurrent-mode efficiency with a smaller drop in both efficiency and output power.

By using concurrent dual-band PAs, the number of PAs and duplexers can be reduced, as well as eliminate the use of duplexers/triplexers, since the loading effect to each other when two PAs are combined for carrier aggregation are insignificant. However, a dual-band duplexer must be provided for the concurrent dual-band PA to be useful in the carrier aggregation in FDD system. The improvement of the whole RF FEM does not come from the improvement in power amplifiers alone, other components in RF FEM should also work together to make it happen.

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